National Research University Higher School of Economics

(HSE University)

Published as a manuscript

Aleksandr Yur'yevich Romanov

METHODS, MODELS, AND ALGORITHMS FOR NETWORK-ON-CHIP DESIGN BASED ON CIRCULANT TOPOLOGIES

SUMMARY OF THE DISSERTATION

for obtaining a scientific degree of a Doctor of Technical Sciences

Moscow

2024

1 Introduction

Relevance of the research topic

Nowadays, system-on-chip design is one of the most rapidly developing areas in microelectronics. More and more demands are made on systems-on-chip in terms of performance, resource costs, power consumption, etc. This leads not only to intensive (by increasing the clock frequency of individual cores) but also to extensive development of systems-on-chip (when cores become tens, hundreds and even thousands) [1, 2], which requires new approaches for more efficient organization of the communication environment between individual cores. Here the experience of designing traditional computer networks comes to the rescue; on its basis, the concept (paradigm) of networks-on-chip is formulated: the network consists of separate complex-functional blocks (CF-blocks) possessing universal interfaces and supporting a single communication protocol; at the same time, they are united by a homogeneous communication environment (communication subsystem) [3]. This allows ensuring reproducibility and scalability of networks-on-chip, predictable throughput and resource and time costs for network design.

The theory and practice of network-on-chip design is continuously evolving and has become very extensive over the past few decades, including a large number of different areas. Particular attention is paid to the design of the network-on-chip communication subsystem, as it is a key component of the network. The design process of the network-on-chip communication subsystem generally consists of defining six basic characteristics of the network [4], such as topology (organization of communication between network elements), routing (determination of data paths in the network), switching (method of data transmission in the network), data flow control (allocation of data channels in the network), buffering (method of intermediate storage of packets), and arbitration (scheduling the use of channels and buffers).

These six main characteristics (among other less important ones) create a large architectural space that defines a huge number of options for network-on-chip organization. This dissertation (within the topological approach) focuses on the first most important characteristic, the topology, as well as on the associated routing, while considering the network communication subsystem optimization problem as a search for optimal network-on-chip topologies.

Network topologies can be classified as physical and logical. Physical topologies are defined by the way the cores are connected in a real chip, and logical topologies are defined by the graph of connections between network nodes [5]. In this case, in logical topologies, simplifications according to which the connections have a unit length and the same throughput, and the nodes of the graph are homogeneous are often taken. Logical topologies of networks- on-chip are characterized by a great variety of graph structures and can be used for testing and search of the best

variants of connections. At the same time, the topology realization during synthesis at the physical level is determined by the algorithms of the synthesizing ECAD of integrated circuits. This allows the designer to abstract from the physical implementation and perform the design and modeling first at a high level and then (if the network meets the design requirements) descend to a lower HDL- model level. The approach in which the design of networks-on-chip is based on a logical topology can be called topological [6].

Networks-on-chip came to replace shared buses [7], when integrated circuit design technologies reached such a level that it became possible to accommodate tens and hundreds of processor nodes on a single chip. At that time, buses, as a communication medium, became too slow and insufficient for transferring huge data streams between individual nodes - primarily due to the fact that when a classical bus is transmitted [8], it can only handle one transmission at a time. This disadvantage is partially mitigated by segmenting buses and using separate additional paths (DMA, streaming interfaces, etc.) [9] serving heavy traffic flows. But this is still insufficient for multiprocessor systems with tens and hundreds of nodes. The concept of networks-on-chip proposed in the early 2000s [2] continues to be relevant now [10]. Its basic idea is to organize transmission on a chip similar to classical communication networks: to divide the communication subsystem into separate short segments over which data is transmitted simultaneously and in parallel (Figure 1). The data transmission is controlled by routers, and communication paths run between the macro-blocks of the network-on-chip [11].

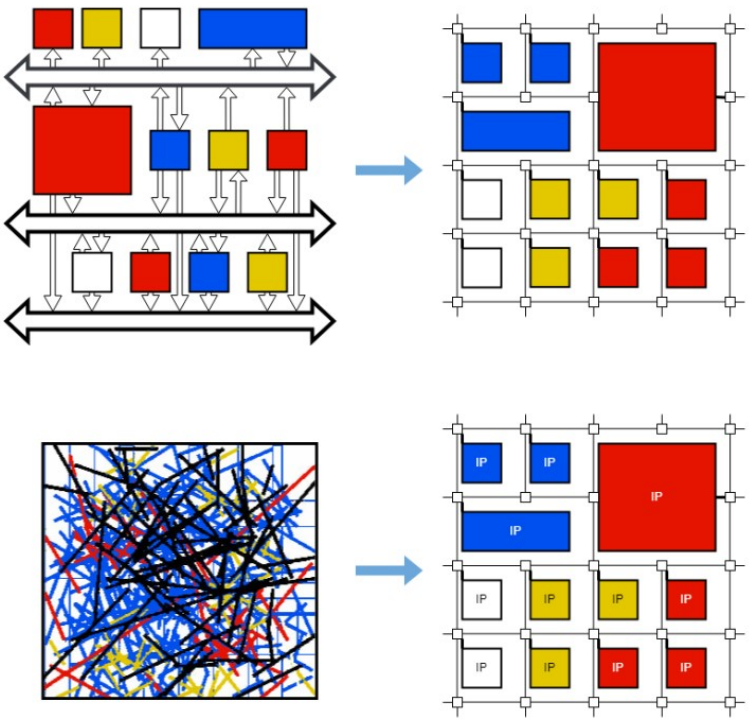


Figure 1 – Classic concept of network-on-chip with mesh topology versus bus topology [12]

In the network-on-chip, it is impossible to directly transfer the multi-layer OSI model [13] from classical communication networks: in general, there is no need to provide data recovery coding, data encryption, the ability to connect new subscribers to the network; and the length of connections is very short, and routers should be very simple. It is possible to establish a correspondence between the OSI layers and the communication subsystem of a network-on-chip [14, 15], but it will not be completely accurate (Figure 2). Communication networks in supercomputers [16, 17] are organized closest to networks-on-chip, but there are peculiarities that do not allow to directly transfer solutions from there to the area of networks-on-chip. This necessitates the development of our own approaches and methods for designing networks on-chip.

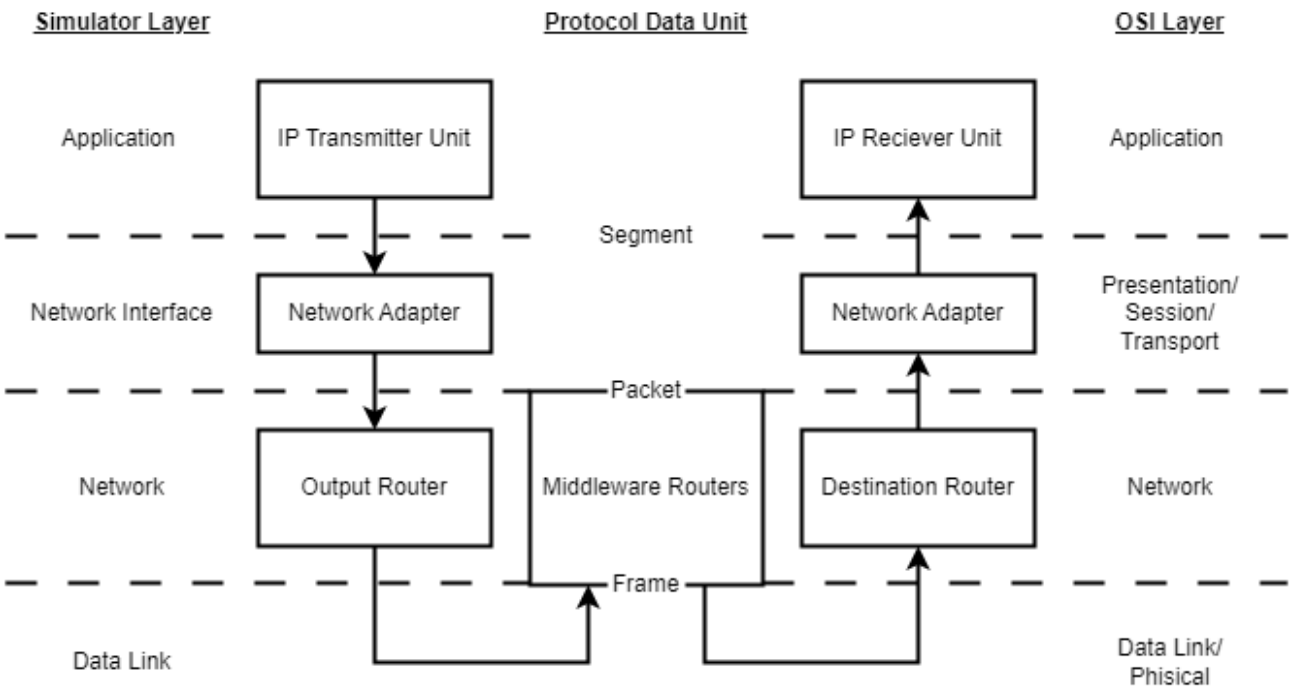


Figure 2 – Correspondence of data transmission in the network-on-chip to the layers of the OSI network model

The idea of organizing the communication subsystem in a network-on-chip in the form of a mesh-like structure turned out to be very convenient, and for a long time, it is the main one in designing networks-on-chip. For example, this is how the communication subsystem is organized in Intel Xeon E5 class processors (it even got the name Intel Mesh Interconnect) [18, 19] or in ET-SoC-1 chip [20] from Esperanto Technologies consisting of 1089+4 64bit – RISC-V processor cores. In addition, due to the imperfection of ECAD tools for integrated circuits synthesis, it is convenient to use simplification during design by representing individual CF-blocks of the network as rectangles compactly arranged on the chip area (Figure 1).

But over time, it became clear that the 2D mesh topology (hereinafter, the most common term without 2D is used, implying it unless something else is indicated: for example, 3D) does not have the best topological characteristics [2*] (first of all, the diameter and average distance between the nodes matter; but the width of the bisection, vertex degree, number of connections, etc. are also important). For this reason, in particular, Intel applies ring topology (for example, in Intel Core i9-9900KS) [21], torus topology (for example, in Ice Lake-SP) [22], and many other topologies in its chips.

In addition, if one looks at the final chip under a microscope, the original cellular structure will hardly be seen. In addition, the simplification that the main connection routes between routers pass between macro-blocks is not true, because the chip is initially multi-layered, and the connections are made on several layers of metallization.

If we take into consideration networks-on-chip on FPGA chips, which reached such sizes that they can accommodate a network with tens and hundreds of nodes [23], we should admit it is even more difficult to maintain the original abstraction with the representation of individual macro-blocks in the form of rectangles (Figure 1) in them – due to the uneven distribution of individual resources on the area of the FPGA chip.

The development of chip design technologies has led to the emergence of 2.5D [24] and 3D [25] networks-on-chip. New technologies have been developed to realize the data transmission path (wireless channel [26], optical channel [27], etc.) at different levels of the chip, which does not allow using mesh as the basic topology of networks-on-chip.

Thus, researchers studying networks-on-chip have gradually come to the general conclusion that sticking to the original idea of representing networks-on-chip as shown in Figure 1 does not make sense; with keeping the concept of short connections between routers, the way routers are connected can be viewed separately as a graph called network topology (not to be confused with chip topology). Simplifications such as an unweighted graph and equal size of the graph vertices can be used. In high-level on-chip network design and modeling, it is not necessary to take into account technology features and sizes of individual catches, as they will be taken into account in the next stage of HDL- network modeling and synthesis, which are performed at the ECAD level. The graph does not have to be mesh [28]. Moreover, mesh topology is not optimal [2*]; and although it is called regular (because the placement of nodes relative to each other and the connections between them can be described by regular rules), it is not homogeneous.

There are other graph structures better suited to be used as a network topology. Many scientists and engineers have proposed (besides mesh) a large number of different variants of topologies [29] (e.g., Spidergon [30, 31], Chordal ring [32], BFT [33], WK-recursive [34],

hierarchical [35, 36], etc.). Circulants occupy a worthy place among them due to the best parameters of the diameter and average distance, as well as the property of symmetry with respect to their vertices. But it is not enough to propose a topology. It is required to develop the methods for synthesizing optimal topologies for specific design requirements, as well as to create efficient, resource-efficient, and error-resistant routing algorithms for these topologies, which determines the **relevance of this dissertation research**; the articles presented in it are primarily devoted to solving these pressing problems.

It should also be noted that the topological approach is widespread and applied in various fields with communication networks [37], since topological properties of networks can be conveniently studied using graph theory (e.g., as in the works [16, 17] on supercomputers). The network transmission delay is determined by the diameter and average distance between nodes in the graph, while the error resilience of the network depends largely on the connectivity of the graph and its bisection width [38]; while the complexity of routing algorithms depends on how symmetric the graph is. This dissertation is based on the topological approach according to which the network-on-chip and routing algorithms in it are considered at a high level of the graph of its topology, abstracting for simplicity from the physical implementation of the network-on-chip.

Degree of development of the topic

Since mesh topology was the basis of the initial idea of on-chip networks, all new solutions for on-chip networks are naturally adapted to it, and other topologies are also compared to it. It is the basis of most high-level [39] and low-level [1*] [40] models of networks-on-chip, dozens of routing algorithms [41], and projection of the problem graph onto the network-on-chip topology [42, 43] are implemented under it. The next most developed topology is torus [44], because it is very similar to mesh and is actually a development of its concept; many solutions for mesh with minor modifications are suitable for torus. But, as a rule, when these topologies are used, they are secondary and taken for granted. In such cases, the design is based on some other aspect of the network-on-chip design (e.g., implementation of an efficient router [45], a method of traffic distribution in the network [46], etc.) through which the improvement of its performance is achieved.

Since the early days of the concept of networks-on-chip, there have been a number of attempts to utilize the topological approach by applying new topologies. In particular, a number of studies propose to use the experience of telecommunication networks, relying on such switching topologies as Benesch, Klose [47], Dragonfly [48], etc., but their advantage manifests itself primarily in the realization of circuit-level switching, which in networks-on-chip is almost completely supplanted by packet-level switching. The idea of using tree-like topologies

(BFT [33, 49], etc.) is also common, but they do not provide the shortest paths in the network and are difficult to implement, because they require different routers. A separate group of scientists has been developing solutions based on close to fractals WK-recursive topology [34, 50] for a long time. A popular idea of hierarchical topologies [35, 51–53] is to combine several topologies together. But all these studies lack systematicity and do not offer a coherent set of solutions at the level of router implementation, communication protocol, routing algorithm, network error control method, etc. to represent a worthy alternative to mesh / torus.

At the same time, the search for new optimal topologies for on-chip networking applications remains a priority and is embodied in a number of dissertations [54] and published works [55–58].

The application of the topological approach can be best illustrated by the example of works devoted to spidergon topology (STNoC). This topology was first presented by a team of scientists from Advanced System Technology Grenoble Laboratory (part of STMicroelectronix) as an evolutionary development of STBus technology and an alternative to mesh topology at the International Symposium on System-on-Chip in 2004 [59]. In the following 10 years, the technology was actively developed. The results of this evolution are reflected in the chapter [31] (included in the book “Designing 2D and 3D Network-on-Chip Architectures” [60]), where the necessity of using new topological solutions in the design of networks-on-chip and the requirements to them are justified, architectural solutions at all OSI layers (router, network interface, connection) are described, decisions on the choice of switching strategy at the packet level, data flow control and other basic functionality of the network are justified, methods of increasing the size of the network (including at the expense of Cartesian product of the base) are developed. All these are supported by integration with appropriate modeling tools at various levels of abstraction and special design tools.

Thus, the authors of the idea of using spidergon topology to design networks on-chip created everything necessary to make it possible to use it. The great achievement (and at the same time the problem) of this approach was that despite the existence of some open-source software solutions, in the final form, the whole technology was implemented as parts of proprietary software by STMicroelectronix. Since the mid-2000s, the number of published works by the group of scientists who dealt with spidergon dramatically decreased. This was probably due to the end of the grant support for the core team (judging by the topics of their publication activity in the future) and the inability to fully continue the development of these developments by outside researchers due to the closed nature of the key solutions. Spidergon is occasionally referenced to [30, 61] (it is already an example of a standard topology for networks-on-chip), but the very idea of using such a regular and symmetric ring topology has not been developed for a long time. STMicroelectronix products

themselves do not mention STNoC technology (as a framework for developing networks-on-chip). Apparently, this solution turned out to be too new for the state of the industry in the 2000s; it turned out to be unclaimed (at that time, for the real production of networks on a chip with a maximum of tens of nodes, mesh was quite enough) and was gradually removed from the company's product line.

As noted by the authors of the idea of using spidergon in networks-on-chip [31], the problem with the topology is that it is a subset of the circulant topology [62], but it is not optimal (i.e., it does not provide the minimum diameter and average distance between nodes); its scalability is a multiple of two, and the recommended ring size does not exceed 16 nodes. For a larger number of nodes, the idea of small worlds is supposed to be used, dividing nodes into several rings connected through special boundary nodes (this approach is called octagon in [30]), which potentially leads to many new problems related to congestion of such nodes [11*], complex routing, etc.

Thus, due to the closeness of a number of solutions, the presence of a whole set of drawbacks in the spidergon topology (which come from the very nature of the underlying graph), the termination of the development of the idea by the group of scientists who proposed it, as well as the difficulties of its development by other researchers, this topology did not become a replacement for mesh. At the same time, the very concept of using completely regular and symmetric graphs (such as circulants) showed its viability and high prospect.

On the other hand, circulant graphs themselves have been known for a long time [63]; their properties, graph families, synthesis methods, and methods of practical application are still being developed. A number of works have repeatedly proposed the use of circular graphs as a topological basis for general-purpose networks [37, 64–66], wireless networks [67], supercomputer networks [16, 17, 68, 69], cyber-physical systems [70], datacenters [71], etc. The commutative properties of circulants have also been studied, and a number of algorithms for accelerated path finding in such graphs have been proposed [3*]. But all these studies are not unified into a single theory and cannot be directly transferred to the design of networks-on-chip.

Therefore, there is an urgent need for research and development of new circulant topologies that would not have the disadvantages of spidergon, but would have the same set of solutions (methods of topology synthesis for any number of nodes, standardized router, routing algorithms, methods of traffic management and combating deadlocks and network errors, as well as support at all stages of modeling and prototyping) that would allow their application in networks-on-chip.

To summarize, let us formulate the main problems which exist in the field of designing network-on-chip communication subsystems and which this dissertation is aimed to solve:

1. Progress in the development of integrated circuit design technologies leads to ever increasing requirements for network-on-chip communication subsystems.
2. At the level of hardware realization of networks on-chip with the number of nodes exceeding several tens, mesh topology is not optimal and does not meet new technological requirements.
3. Modern means of the integrated circuit design cycle no longer require manual planning of the placement of blocks on the chip, and topologies should be considered primarily as graphs; improving their topological properties leads to improved characteristics of networks-on-chip.
4. The torus topology, as a development of mesh, no longer provides a spatial arrangement of links in the plane and yet retains a number of the drawbacks of mesh.
5. Most of the developed routing algorithms, traffic management algorithms, network-on-chip models, etc. are focused on mesh and torus topologies; other topologies do not have all the necessary tools to be directly used for designing networks-on-chip.
6. Due to the peculiarities of networks-on-chip (data transmission in communication channels is almost instantaneous, no interference, no need to encrypt data, simplified routers, no need to implement the full OSI model, no need to dynamically change the network structure), no solutions from other kinds of communication networks can be directly used in them.
7. The lack of unified approaches and design routes, as well as unified ECAD systems for the development of networks-on-chip, dictates (within the framework of the strategy of import substitution and the development of the Russian electronics industry) the need to develop open ECAD systems for the design of networks-on-chip.

The application of a topological approach to the design of networks-on-chip in which circulant graphs are used as the topology of the communication subsystem solves these problems and is a new scientific and practical field in networks-on-chip.

Aims and objectives of the study

The aim of this dissertation is to increase the throughput and reduce the hardware costs of networks-on-chip by developing a new direction for designing networks-on-chip based on a topological approach using circulant topologies.

To achieve this goal, it was necessary to solve the following problems:

1. Development of methods and tools for synthesizing optimal circulant topologies according to the criteria of reducing the average distance between the nodes and diameter.
2. Comparative analysis of new topologies with classical regular topologies in the context of their application to the problems of network-on-chip design.
3. Analysis of optimal circulant topologies to identify families of circulant topologies and dependencies of graph characteristics on their parameters.
4. Developing tools for high-level and low-level modeling and prototyping of network-on-chip based on circulant topologies.
5. Developing routing algorithms for different families of circulant topologies and comparing them with other algorithms and topologies in terms of average distance, throughput, chip resource consumption, etc.
6. Development of methods for traffic management and control of deadlocks and failures in networks-on-chip with circulant topologies.

Research Methods

The development of a new approach to the design of networks-on-chip based on the application of topological approach using circular graphs is based on the application of fundamental concepts of general graph theory, communication networks, networks-on-chip, modeling and information analysis.

Theoretical and practical significance

Theoretical significance of the dissertation consists in the fact that for the first time, the application of topological approach based on the use of optimal circulant topologies to the design of networks-on-chip is systematically considered. The use of interdisciplinary approach allowed to transfer the achievements in related scientific fields from graph theory, communication networks, modeling and information analysis to the design of networks-on-chip.

For the first time, the concept of topological approach is introduced in relation to the design of networks-on-chip, and its validity for achieving better performance of networks-on-chip is substantiated on the example of standard and new topologies.

The methodology of synthesis of optimal circulant topologies for specific parameters of the designed network-on-chip was developed, which allowed to create the most complete dataset of

optimal circulant graphs for a wide range of orders and dimensions, to describe their characteristics and dependencies, as well as to compare them with other topologies used in networks-on-chip.

New routing algorithms in networks-on-chip based on circulant topologies which rely on different heuristic approaches, mathematical methods, topological methods, relative addressing methods, etc. are proposed.

Methods for controlling data transmission in networks-on-chip providing deadlock and error control in networks-on-chip with circulant topologies were developed.

All new results obtained by the author of the dissertation and stated in the presented articles and patents are of high importance for the development of the theory of network- on-chip design, practical application of circulant topologies, and development of systems for automated design and modeling of networks-on-chip.

2 Scientific results and published works

The new results are as follows:

1. The new direction in network-on-chip design based on the use of circulant topologies, increasing the throughput and reducing hardware costs [1*, 2*, 3*, 4*, 5*, 6*, 7*, 8*, 9*, 10*, 11*, 12*].
2. The algorithm for calculating the shortest paths in a circulant graph and methods for accelerating the procedure for enumerating graph signatures to speed up calculations up to 35,000 times and reduce the dependence of memory consumption on the number of nodes from quadratic to linear compared to classical search methods, due to which it became possible to synthesize a set of optimal circulant graphs with order up to 1000 and dimension up to 10 [8*].
3. For problems of application in networks-on-chip, it makes sense to search for optimal circulant graphs among a subset of ring circulants, which makes it possible to reduce the number of degrees of freedom of the search procedure by 1 [2*].
4. The dataset of optimal circulant graphs, which allows (using mathematical methods and machine learning methods) obtaining estimates of the characteristics of circulant graphs for the parameters given [8*].
5. New and adapted existing models of networks-on-chip of different levels of abstraction, which made it possible to conduct a comparative analysis of the results of modeling circulant and other topologies of networks-on-chip, as well as implement various routing algorithms and combat deadlocks and errors in networks, thereby confirming the advantages of the new solutions proposed [1*, 2*, 3*, 4*, 5*, 6*, 7*, 9*, 11*, 12*].

6. Deterministic quasi-optimal and optimal one-step and multi-step routing algorithms for various families of circulant graphs, which made it possible to perform traffic routing in networks-on-chip based on circulant topologies [2*, 3*, 4*, 5*].
7. The adaptive routing algorithm for various families of circulant graphs, which made it possible to perform traffic routing in networks-on-chip based on circulant topologies under error conditions [6*, 7*].
8. The routing algorithm based on self-organization and relative addressing, which made it possible to route traffic in networks-on-chip in conditions of failure of individual nodes or network connections [12*].
9. The method for managing deadlock-free data transmission in networks-on-chip based on circulant topologies through the use of an additional acyclic subnet which allows bypassing blocked areas in the main communication network [9*].
10. The method for managing deadlock-free data transmission in networks-on-chip based on circulant topologies through the use of virtual channels and decomposition of the topology graph into subnets, making mutual blocking of packets impossible [9*, 10*].

Credibility, novelty and personal contribution of the author

All the results presented are new. For the first time, a new direction in designing networks-on-chip through the use of circulant graphs as their topological basis was proposed and justified. For a new class of networks-on-chip based on circulant topologies, new methods for synthesizing circulant graphs with given characteristics, new models of networks-on-chip of different levels of abstraction, new routing algorithms of different levels of resource consumption, adaptability and error tolerance, as well as new methods for traffic flow control were created to combat deadlocks. It was shown that such networks have better throughput and lower hardware costs compared to networks based on classical regular topologies. The results presented have a formal mathematical proof or are confirmed by the results of high-level modeling, HDL modeling and prototyping.

Scientific novelty of the results obtained:

1. The new direction in the networks-on-chip design is proposed; it differs from the known ones in that the design is based on a topological approach which underpins the use of circulant graphs as the topology of a network-on-chip, thereby increasing throughput and reducing hardware costs on organizing the network-on-chip communication subsystem.
2. The new algorithm for calculating shortest paths and methods for accelerating the procedure for enumerating graph signatures were developed; they (in contrast to other ones) take into account the properties of circulant graphs, which made it possible to speed up calculations

and reduce memory consumption, thereby synthesizing a set of optimal circulant graphs with order up to 1000 and dimension to 10.

3. New models of networks-on-chip of different levels of abstraction were developed and adapted; they (in contrast to other ones) support circulant topologies and are combined into a single integrated ECAD system, which made it possible to conduct a comparative analysis of the results of modeling circulant and other topologies of networks-on-chip, as well as implement various routing algorithms and deal with deadlocks and errors in networks, thereby confirming the advantages of the proposed new direction in network-on-chip design.
4. New routing algorithms were developed; they (in contrast to the existing ones) take into account the properties of circulant graphs, as well as the features of their implementation at the hardware level, which made it possible to provide traffic routing in various configurations and for various requirements for the operation of networks-on-chip with circulant topologies.
5. New methods for managing data transmission in networks-on-chip were developed; they (in contrast to the existing ones) take into account the properties of circulant graphs and provide deadlock-free routing through the use of the additional acyclic subnet or use of virtual channels and decomposition of the topology graph on the subnet.

The practical significance of the results obtained is that:

1. The proposed new direction in network-on-chip design based on the use of circulant topologies opens developers a wider choice of technical solutions and approaches for the design taking into account all the requirements and restrictions imposed by the specific task of network-on-chip design and operating conditions.
2. Software tools for the synthesis of optimal circulant graphs with given parameters were developed.
3. The dataset of optimal circulant graphs was created; using mathematical methods and machine learning methods, it allows obtaining estimates of the characteristics of circulant graphs for given parameters, as well as searching and studying new families of circulant graphs.
4. The developed new and adapted existing models of networks-on-chip of different levels of abstraction, as well as prototyping tools based on them, represent a single integrated ECAD system that implements the high-level design stage and is combined with the stages of logical and physical synthesis, forming a single end-to-end route for network-on-chip design.

5. The developed new routing algorithms and methods for controlling data transfer in networks-on-chip make it possible to ensure routing of traffic in various configurations and for various operating conditions of networks-on-chip with circulant topologies, including uneven load distribution, presence of deadlocks, failure of network nodes, etc.

Materials of the dissertation were published in 50 printed works, 16 of them – in peer-reviewed journals (7 – Q1 Scopus, 9 – Q2 Scopus, 5 – Q1 WoS, 10 – Q2 WoS), 12 articles in VAK/RSCI journals (C, D list), 24 – in conference proceedings. 7 certificates for computer programs were obtained.

The dissertation is protected by 10 Q1–Q2 Scopus/WoS articles, 1 VAK/RSCI article and 1 article in the proceedings of a leading international conference (Scopus).

Approbation of the obtained results

The main results of the dissertation research were personally presented by the author of the dissertation at the following international and specialized conferences:

1. Report “SystemC NoC Simulation as the Alternative to the HDL and High-level Modeling”, 18th FRUCT & ISPIT Conference, April 2016, St. Petersburg, Russia.
2. Paper “Application of exhaustive search, branch and bound, parallel computing and Monte-Carlo methods for the synthesis of quasi-optimal network-on-chip topologies”, 2017 IEEE East-West Design & Test Symposium (EWDTS), October 2017, Novi Sad, Serbia.
3. Report “Development of routing algorithm in networks on-chip with multiplicative circulant topology”, Problems of development of advanced micro- and nanoelectronic systems (MES-2018), October 2018, Zelenograd, Russia.
4. Paper “Routing in Networks-on-Chip with Circulant Topology with Three Generatrices of Type C(N;S1,S2,S3)”, IEEE 2019 International Russian Automation Conference (RusAutoCon), September 2019, Sochi, Russia.
5. Paper “Fault-Tolerant Routing in Networks-on-Chip Using Self-Organizing Routing Algorithms”, 47th Annual Conference of the IEEE Industrial Electronics Society (IECON), October 2021, Toronto, Canada.
6. Paper “Optimal Routing Algorithm in Dense Gaussian Networks-on-Chip”, IEEE 2nd International Conference on Electrical, Computer, Communications and Mechatronics Engineering (ICECCME), November 2022, Maldives.

The results of the dissertation formed the basis of the following scientific research works, performed in co-authorship:

1. Academic Fund Program project of the HSE University “Design of networks-on-chip based on circulant topologies”, No. 18-01-0074, 2018–2019.
2. Basic Research Program project of the HSE University “Synthesis of circulant topologies for application in networks-on-chip”, R&D reg. no. AAAA-B19-219042690141-3, 2018.
3. Basic Research Program project of the HSE University “Modeling of networks-on-chip with communication subsystem based on circulant topologies”, R&D reg. no. AAAA-B20-220051590048-4, 2019.
4. Basic Research Program project of the HSE University “Development of a hybrid model for design and simulation of networks-on-chip”, R&D reg. no. AAAA-B21-221011990285-2, 2020.
5. Basic Research Program project of the HSE University “Development of routing algorithms in networks-on-chip”, R&D reg. no. 222030100043-1, 2021.
6. Basic Research Program project of the HSE University “Research of new promising topologies and routing methods for application in networks-on-chip”, R&D reg. no. 223020200338-7, 2022.
7. Basic Research Program project of the HSE University “Automation of network-on-chip modeling”, R&D reg. no. 123020800124-1, 2023.
8. Basic Research Program project of the HSE University “Research of new classes of circulant graphs and their characteristics for designing networks-on-chip”, 2024.
9. RSF project “Self-organization in networks-on-chip: principles, models, routing algorithms, programs, and development technologies”, No. 22-29-00979, R&D reg. no. 122031400059-7, 2022-2023.

The results of the dissertation, in particular, the developed means of prototyping large-scale projects (including networks-on-chip) with the help of a hardware-software -complex based on several FPGAs were considered by leading specialists of LLC "KNS GROUP" (YADRO - Group of Companies) as a result of which a decision was approved to recommend the above results for use by industry leaders in the development of prototyping tools for multiprocessor systems in order to reduce hardware costs and accelerate the process of debugging multiprocessor systems.

The results of the dissertation work are implemented in the educational process of the Department of Computer Engineering of MIEM of the National Research University Higher School

of Economics during the training of bachelors in the direction of 09.03.01 “Computer Science and Computer Engineering”, namely, in the teaching of disciplines: “Design of systems on a chip”, “High-level and simulation modeling of digital systems”, “System design of digital devices”, as well as in the implementation of projects by students of 2-4 courses in the framework of project activities.

List of articles on the topic of dissertation submitted for the protection:

[1*] Romanov, A.; Ivannikov, A. SystemC Language Usage as the Alternative to the HDL and High-Level Modeling for NoC Simulation. *Int. J. Embed. Real-Time Commun. Syst.* **2018**, doi:10.4018/IJERTCS.2018070102. (Q2 Scopus, Q4 WoS)

https://www.igi-global.com/article/systemc-language-usage-as-the-alternative-to-the-hdl-and-high-level-modeling-for-noc-simulation/204481

[2*] Romanov, A.Y. Development of Routing Algorithms in Networks-on-Chip Based on Ring Circulant Topologies. *Heliyon* **2019**, 5, e01516, doi:10.1016/j.heliyon.2019.e01516. (Q1 Scopus, Q1 WoS)

https://www.sciencedirect.com/science/article/pii/S2405844018355208

[3*] Monakhova, E. A.; Romanov, A. Y.; Lezhnev, E. V. Shortest Path Search Algorithm in Optimal Two-Dimensional Circulant Networks: Implementation for Networks-on-Chip. *IEEE Access* **2020**, 8, 215010-215019, doi:10.1109/ACCESS.2020.3040323. (Q1 Scopus, Q2 WoS).

https://ieeexplore.ieee.org/document/9268938

[4*] Romanov, A.Y.; Lezhnev, E. V.; Glukhikh, A.Y.; Amerikanov, A.A. Development of Routing Algorithms in Networks-on-Chip Based on Two-Dimensional Optimal Circulant Topologies. *Heliyon* **2020**, 6, e03183, doi:10.1016/j.heliyon.2020.e03183. (Q1 Scopus, Q1 WoS)

https://www.sciencedirect.com/science/article/pii/S2405844020300281

[5*] Romanov, A.Y.; Starykh, V.A. Routing in Triple Loop Circulants: A Case of Networks-on-Chip. *Heliyon* **2020**, *6*, e04427, doi:10.1016/J.HELIYON.2020.E04427. (Q1 Scopus, Q2 WoS).

https://www.sciencedirect.com/science/article/pii/S2405844020312718

[6*] Monakhov, O. G.; Monakhova, E. A.; Romanov, A. Y.; Sukhov, A. M.; Lezhnev, E. V. Adaptive Dynamic Shortest Path Search Algorithm in Networks-on-Chip Based on Circulant Topologies. *IEEE Access* **2021**, *9*, 160836-160846, doi:10.1109/ACCESS.2021.3131635. (Q1 Scopus, Q2 WoS).

https://ieeexplore.ieee.org/document/9628133

[7*] Monakhova, E.A.; Monakhov, O.G.; Romanov, A.Y. Routing Algorithms in Optimal Degree Four Circulant Networks Based on Relative Addressing: Comparative Analysis for Networks-on-Chip. *IEEE Trans. Netw. Sci. Eng.* **2023**, *10*, 413-425, doi:10.1109/TNSE.2022.3211985. (Q1 Scopus, Q1 WoS).

https://ieeexplore.ieee.org/document/9910381

[8*] Romanov, A. The Dataset for Optimal Circulant Topologies. *Big Data Cogn. Comput.* **2023**, 7, 80. doi: 10.3390/bdcc7020080. (Q2 Scopus, Q1 WoS)

https://www.mdpi.com/2504-2289/7/2/80

[9*] Romanov, A.Y.; Myachin, N.M.; Lezhnev, E.V.; Ivannikov, A.D.; El-Mesady, A. Ring-Split: Deadlock-Free Routing Algorithm for Circulant Networks-on-Chip. *Micromachines* **2023**, 14, 141. doi: 10.3390/mi14010141. (Q2 Scopus, Q2 WoS).

https://www.mdpi.com/2072-666X/14/1/141

[10*] El-Mesady, A.; Romanov, A.Y.; Amerikanov, A.A.; Ivannikov, A.D. On Bipartite Circulant Graph Decompositions Based on Cartesian and Tensor Products with Novel Topologies and Deadlock-Free Routing. *Algorithms* **2023**, 16, 10. doi:10.3390/a16010010. (Q2 Scopus, Q2 WoS)

https://www.mdpi.com/1999-4893/16/1/10

[11*] Romanov, A. Yu. Investigation of networks on-chip with mesh topology using the NoCTweak model. *Information Technologies* **2016**, 22, 7. 498-503. (VAK/RSCI, D list)

http://novtex.ru/IT/it2016/it716_web-498-503.pdf

[12*] Romanov, A.; Myachin, N.; Sukhov, A. Fault-Tolerant Routing in Networks-on-Chip Using Self-Organizing Routing Algorithms. *Proceedings of IECON 2021 - 47th Annual Conference of the IEEE Industrial Electronics Society*; IEEE, **2021**. doi: 10.1109/IECON48115.2021.9589829. (n/q Scopus, n/q WoS).

https://ieeexplore.ieee.org/document/9589829

3 Summary of work. Main results

The main results of the dissertation are logically divided into 4 parts reflecting all the necessary elements to enable the design of networks-on-chip based on circulant topologies:

1. Methods and tools for synthesizing optimal circulant topologies according to the criteria of reducing the average distance between nodes and diameter.

2. Modeling and prototyping tools for on-chip networks that support circulant topologies.

3. Deterministic and adaptive routing algorithms for different families of circulant topologies as applied to networks-on-chip.

4. Methods for traffic management, deadlock and error control in networks-on-chip with circulant topologies.

3.1 Synthesis of circulant topologies

A circulant graph (circulant network) [72] is a graph consisting of a set of vertices $V = \{0, 1, \dots, N-1\}$ and edges $E = \{(v, (v \pm s_i) \bmod N) | v \in V, i = \overline{1,k}\}$. The signature of a circulant graph (parametric description) has the form $\mathrm{C}(N;\ s_1, s_2, \dots,\ s_\mathrm{k})$, where N - the number of vertices, $1 \le s_1 < s_2, < \dots, < s_k \le N/2$ - formers of the circulant graph, k - its dimension.

The generators of a circulant graph determine the steps of transitions between neighboring vertices of the graph. For example, the signature $\mathrm{C}(27; 1,4,7)$ defines the graph shown in Figure 3.

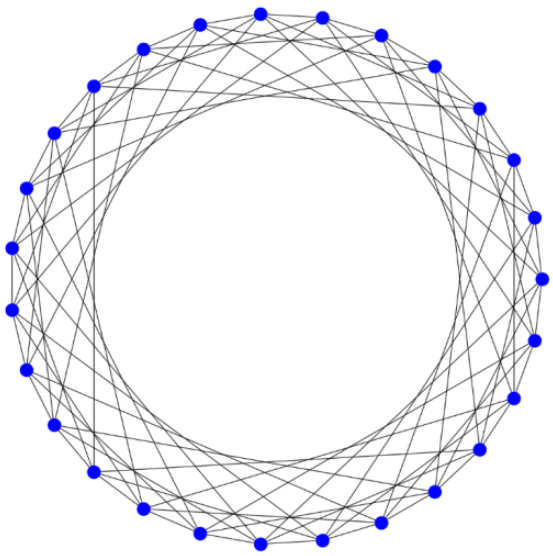


Figure 3 – Circulant graph $\mathrm{C}(27; 1,4,7)$

The diameter and average distance of shortest paths (as well as the bisection width) are among the main topology parameters that determine the efficiency of the data transmission system. A circulant graph with minimum diameter and average distance at given graph order and dimensionality is optimal [17].

One of the problems of circulant synthesis is the search for families of optimal graphs with the number of nodes greater than 100 and degree of vertices greater than 4 [73]. Much attention is paid to the search for analytical descriptions of the results of calculations of static parameters of graphs. Thus, in [74] a series of parametrically described infinite families of circulant networks of degree six was obtained, which made it possible to develop general analytical methods for finding the shortest paths of circulant graphs. And in [75], formulas for computing the diameter of them were presented. In [24–26] families of two-dimensional optimal circulants were found, and in [27] families of circulants of different degrees greater than 6 were analytically described. It is possible to synthesize some families of graphs by applying various mathematical operations on graphs [76–78]. In [79] a table which allows to compute the diameter of circulant graphs of class $\mathrm{C}(N;\ 1, s_1)$ using formulas (which is also a significant result in the field of analytic formulas) was presented.

Analytical descriptions of families of optimal graphs given in various studies do not cover all possible variants of optimal circulant graphs for different optimality criteria and graph parameters. The search of optimal graphs for engineering and scientific applications is proposed to be carried out by software tools.

Using directly the exhaustive search method (when different signatures of circulants are sequentially searched, each of them is characterized, and the best ones are selected according to the given criteria, taking into account a certain order and dimensionality) is not possible with modern computational means, due to a sharp increase in the number of search variants, as well as the complexity of the procedures for calculating the diameter, average distance, bisection width, etc.). This problem is NP-hard [17, 80], and even the use of a high-performance cluster [16] is not sufficient. Therefore, the exhaustive search method [81, 82] was supplemented with methods of parallelization of computations, the method of branches and bounds, as well as heuristic rules based on the use of symmetry and regularity properties of circulant graphs.

The first basic prototype of the software that allowed to obtain the first series of generated graph signatures was presented at the ELNANO conference in 2018 [80] and then continuously developed until a stable version of the software was presented in [8*] with the help of which (and its previous versions) an extensive dataset of optimal circulant graphs with order up to 1000 and dimension up to 10 over a period of 7 years was obtained. The software is hosted in an open source repository and can be used by other researchers; it can also be used to additionally generate new

signatures for specific requirements of the resulting graph. The structure of the circulant graph signature generation application is shown in Figure 4.

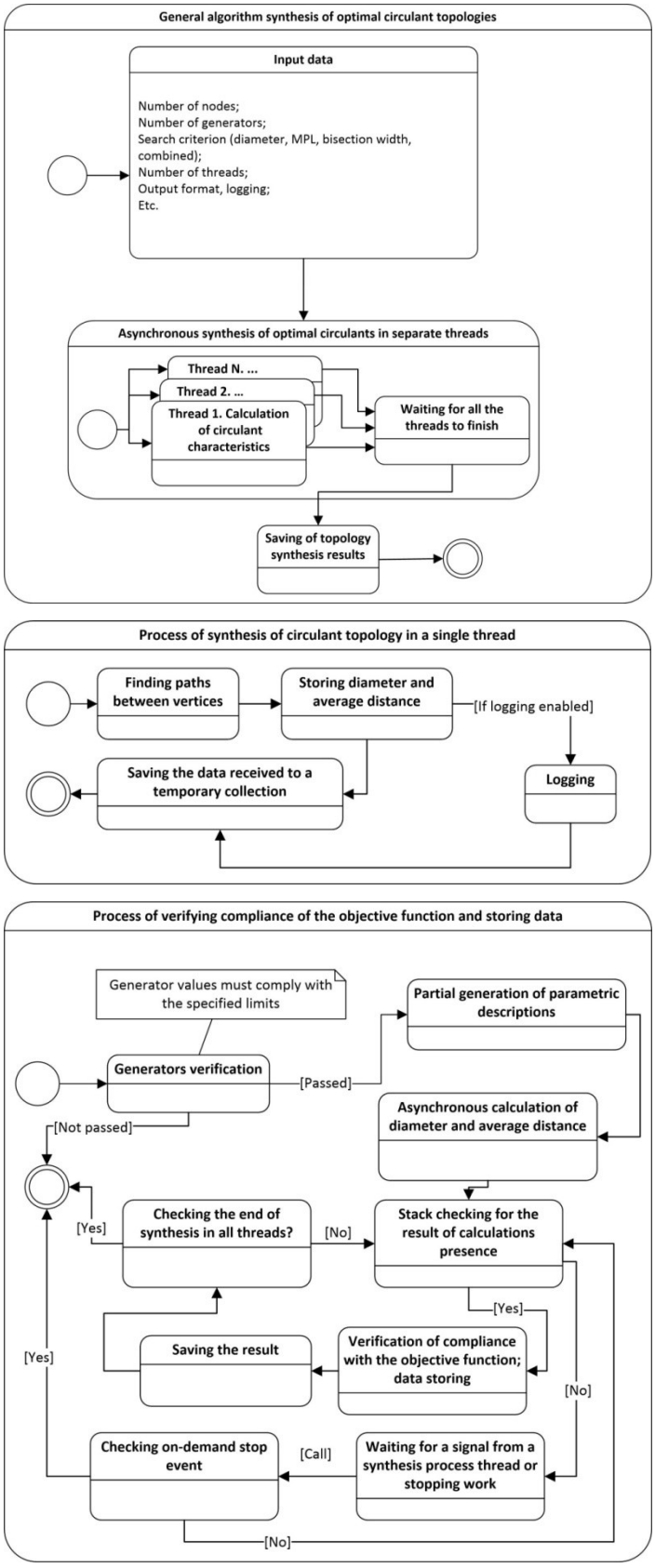


Figure 4 – Software structure for generating circulant graph signatures

The acceleration of the procedure for finding signatures of circulant graphs was performed in two planes: on the basis of the properties of the graphs themselves due to which the number of candidate signature variants is reduced, and also due to the acceleration and reduction of resource requirements for the execution of the graph diameter search algorithm.

Let us analyze the methods of search acceleration with respect to the problem under consideration. Let us denote the topology generators $(1 \leq s_i < N) \in S$ [63], where N – the number of nodes, k – graph dimension (number of generatrices), $i = 1, \dots, k$. If we take the value of the image, which is greater than N, then in this case there will be created repeated parametric descriptions of the topology corresponding to the descriptions of $C(N;\ s_1\%N, s_2\%N, \dots, s_k\%N)$, where $s_i \geq N$. If we discard them, we are left with $(N-1)$ of k variants of possible topologies.

Another feature of circulant graphs is that circulant topologies with different parametric descriptions, for example, $C(10;\ 2, 1)$ and $C(10;\ 1, 2)$, are the same [72]. To eliminate such repetitions, we introduce the condition $1 < s_1 < s_2 < \dots < s_k < N$ (the generators are ordered in ascending order; there are no repeating generators), which leads to the reduction of unnecessary repeated checks of topologies.

Another step to reduce the number of overshoots is to use the isomorphism of circulant topologies of type $C(N;\ s_1, \dots, s_i, \dots, s_k)$ and $C(N;\ s_1, \dots, N - s_i, \dots, s_k)$ [72]. This property allows us to restrict ourselves to the enumeration of the values of the generators $s_k < N/2 + N\%2$ (Figure 4).

Taking into account the properties of circulant topologies in the algorithm realizing an exhaustive search, the number of repetitions can be significantly reduced, and the number of iterations in general is the value $\approx (N/4 + 1/2)^k$, which leads to the reduction of the time of topologies search up to 10000 times.

For most regular topologies, such as mesh, hypercube [83], torus, the calculation of diameter and average distance is performed using formulas that depend on the number of nodes [44]. Circulant topology is determined by the graph order and the lengths of the generators, so there are no universal formulas for calculating the diameter and average distance. In most cases, one can only estimate the maximum lower and upper bounds of these parameters [62], but there is no way to compute the exact values of these metrics for specific instances of topologies. Only for some classes of circulants (such as two-dimensional circulants), there are formulas for finding optimal topologies [84, 85]. Therefore, for each generated topology, it is necessary to find the diameter and average distance as for a usual irregular topology (Figure 4). For some families of circulants (for

example, for two-dimensional circulants [62, 79, 86–88]), there are fast algorithms for computing some characteristics, which are used in the developed software. But for the general case, it is required to use Dijkstra's algorithm [89] (due to its simplicity, it is used in [80]), A*[90], and others. Since circulant topologies can be described in terms of circulant matrices, a subspecies of Teplitz matrices [91], it suffices to find all the paths from any one vertex to other vertices. The diameter of the graph in this case corresponds to the largest distance between vertices, and the average distance corresponds to the arithmetic mean of these paths [92].

The classical Dijkstra algorithm [89] operates with adjacency matrices and is a sequential search in width. This leads to the fact that the search procedure is rather long and requires significant memory consumption for large-order graphs. Therefore, the search algorithm was modified by representing the graph as an array of its generators, with intermediate distances between vertices stored in the array as well. This accelerated the algorithm up to 3.5 times and made it possible to bring the dependence of memory consumption on the number of nodes from quadratic to linear. All these, together with the speedup obtained by reducing the search variants, resulted in speeding up the final procedure of searching for optimal circulant topologies up to 35,000 times.

3.2 Dataset of circulant topologies

The developed software was used to create a dataset of optimal circulant graphs [8*] and means for storing and processing data of this kind [93, 94]. It can be used to check other synthesis algorithms [16, 17, 95], as well as analytical formulas [79, 88, 96], to describe the characteristics of circulant graphs.

The study of the resulting dataset allows us to assert that it makes sense to search for optimal circulant graphs for application problems in networks-on-chip among a subset of ring circulants [72], since in most cases, there is a ring circulant among the optimal circulants for a certain number of nodes. But even if it does not exist, there will be found an optimal ring circulant whose characteristics will be close ($\mathrm{PPMC} \to 1, \mathrm{MAE} \to 0$) to the maximum optimal circulant (Figure 5) [2*] [97]. If this difference is neglected, we can reduce the number of degrees of freedom of the search procedure by 1. Also, the obtained dataset allows us to prove the advantage of circulant topologies over mesh and torus topologies.

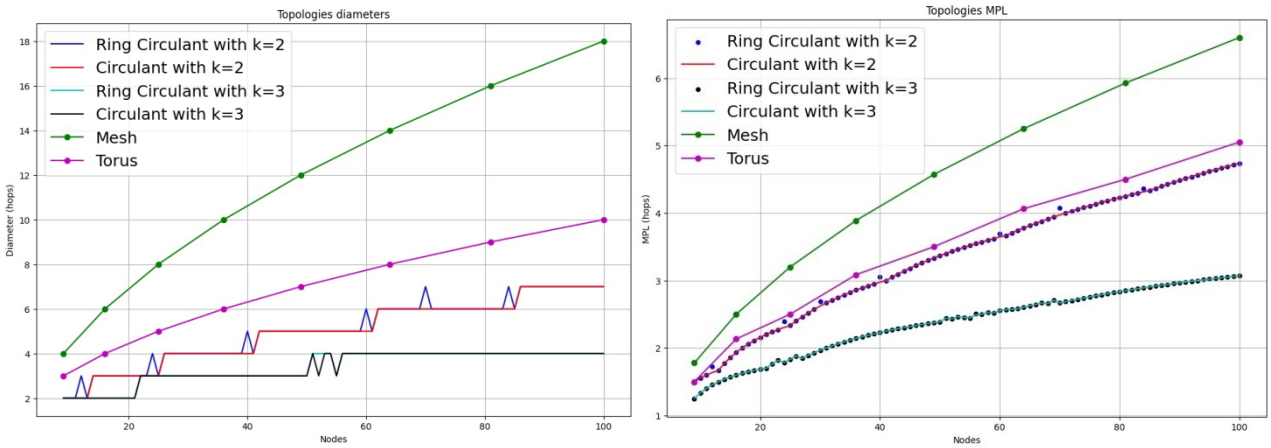


Figure 5 – Comparison of the characteristics of ring and marginal optimal circulant graphs of order 2 and 3 and mesh and torus square graphs

The created dataset can be used to identify regular dependencies between the characteristics of graphs (the diameter, average distance, lengths of formers, bisection width) and number of their vertices, dimension, etc. [8*]. In addition, the generated dataset can be employed to train machine learning models [98] to predict graph characteristics. The representation of the generated topologies as a dataset opens a wide range of possibilities for studying optimal circulant graphs, as well as for finding new families and formulas for estimating their characteristics. The search for new families of circulant graphs is an actual and open problem, and the obtained dataset is the first of its kind and serves as a model for the development of similar datasets by other scientists [96].

3.3 Modeling and prototyping of networks-on-chip

The network-on-chip design can be divided into several main sequential stages [15, 99]: specification, preliminary design, high-level modeling, low-level modeling, prototyping or cosimulation, and synthesis of the integrated circuit of the network-on-chip. As the experience of implementation and development of spidergon topology [31] shows, it is important that each stage has its own open-source tools and that they are united by a common interface and data transfer formats between different design stages to ensure the principle of end-to-end network-on-chip design.

The specification and preliminary design stages are beyond the scope of this paper and involve the use of standards and tools for organizing document flow within the company's ERP system. At these stages, the requirements for the network-on-chip are formulated and preliminary decisions are made on the choice of how the network will be organized.

The stages of high-level and low-level modeling are still not fully formalized. There are hundreds of high-level [11*] [39] and dozens of low-level [1*] [40] models of networks-on-chip

designed to study and analyze various aspects of networks-on-chip. They differ in both description languages and accuracy, as well as in sets of input parameters and characteristics under study.

The prototyping stage is closely related to low-level modeling, because it is an implementation of the HDL model of the network-on-chip on FPGA, which allows thousands of times faster modeling and more accurate investigation of signal changes at the chip level [1*]. The complexity of the problem is that the resources of the FPGA chip are significantly limited, which makes it impossible to accommodate a large size network-on-chip on it. This problem is solved by dividing the network-on-chip into several FPGA chips or by separately modeling different parts of the FPGA [100].

The network-on-chip integrated circuit synthesis stage is described and implemented by the same tools as for integrated circuit design. Here, there are both proprietary software products (e.g., IC Design compiler) [101, 102] and open-source products (OpenROAD et al.) [103, 104].

The unified route of on-chip network design ensuring the implementation of the principle of end-to-end design is proposed to be implemented in the format of integrated ECAD whose generalized architecture is presented in Figure 6.

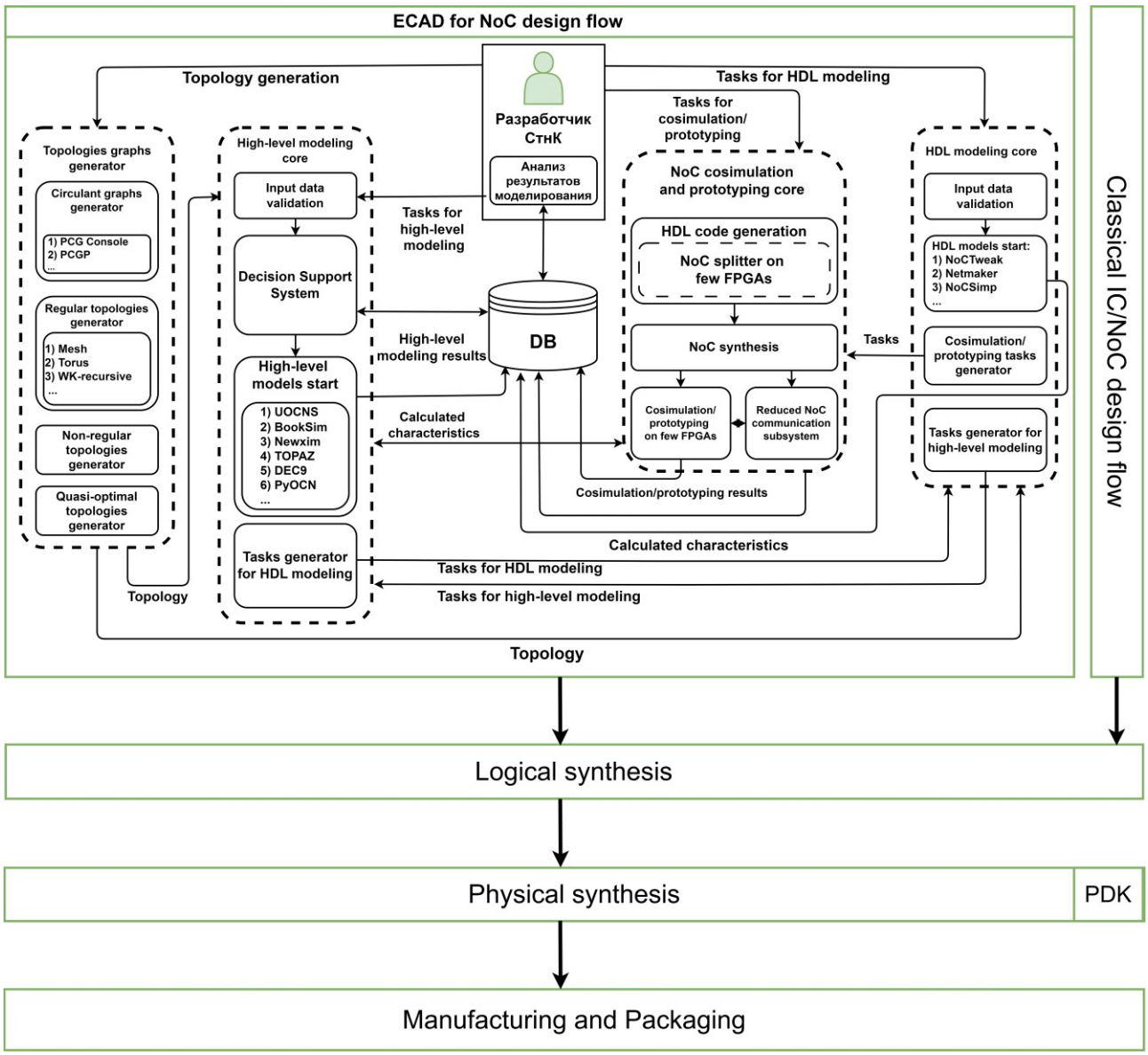


Figure 6 – Generalized ECAD architecture for the implementation of a single route for designing a network-on-chip

Within the framework of the proposed ECAD architecture [101], the author developed the new [1*, 9*] [106] and adapted existing [11*] [107–109] network-on-chip models of different abstraction levels; the author also created the tools for prototyping networks-on-chip [100, 110–112] and described the unified data transfer formats between different stages of network-on-chip design [113, 114]. This allowed us to conduct a comparative analysis of the results of modeling circulant and other topologies of networks-on-chip, as well as implementations of various routing algorithms [2*, 3*, 4*, 5*, 6*, 7*] preventing deadlocks [9*, 10*] and failures in the network [12*] due to which we can confirm the advantages of the proposed new solutions.

3.4 Deterministic routing algorithms

The main problem in the development of new topologies for networks-on-chip is that in addition to the topology, it is necessary to develop a sufficient number of different routing

algorithms that would satisfy the requirements for simplicity, adaptability, optimality, resource consumption, and so on. During 20 years of development of the theory of network-on-chip design for mesh and torus topologies, researchers proposed several hundreds of different routing algorithms [41, 115–117]. For spidergon [31], WK-recursive [118], hierarchical topologies [119], etc., there are their own algorithms.

At the same time, the methods and approaches to routing used in classical communication networks cannot be directly transferred to the network-on-chip. The communication subsystem of the network-on-chip, which is based on routers whose classical scheme is shown in Figure 7 can consume up to 40% of chip power consumption and up to 30% of resources [120].

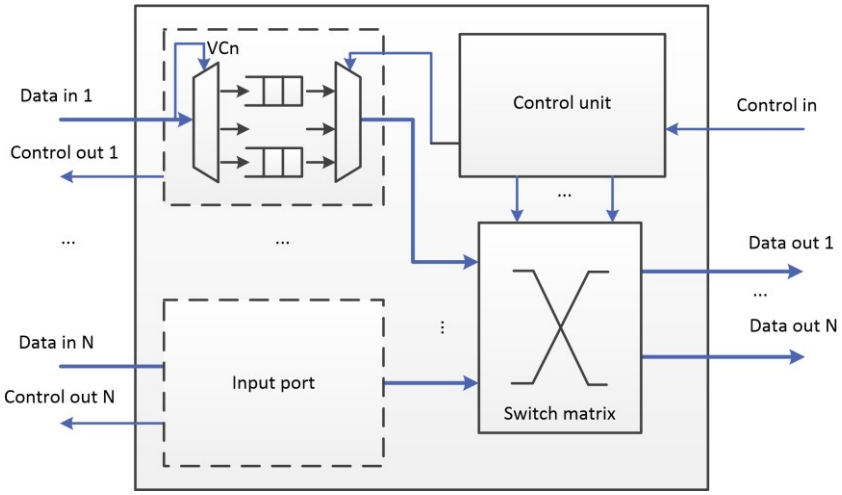


Figure 7 – Classical scheme of a network-on-chip router

The route of packet movement can be calculated in advance in the computational node or stored in a specialized table and then written into the head flit of the packet before sending it to the network. Then the implementation of the router will be minimal - it will be enough to count the next step and direct the packet to the appropriate port (Figure 8). But this approach is too redundant and requires a lot of computational resources or memory. Therefore, in a network-on-chip, the packet path determination is usually performed in the router itself.

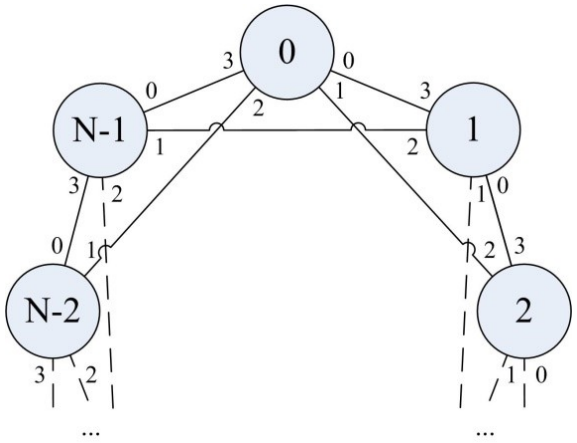


Figure 8 – Example of router port numbering in a network-on-chip [2*].

The simplest and most obvious method, table-based routing, is described in [2*]. A packet in the head flit contains the destination node number. Each router stores a list of ports where a packet must be routed to reach the corresponding node. Since circulants are completely symmetric with respect to their vertices [72], the table will be identical for all nodes, while only storing information for the right half of the ring. In addition, adjacent nodes on a chip can share a common routing table. Nevertheless, even with these improvements, this approach leads to an excessive consumption of chip memory resources [4*].

In [2*] another routing algorithm called “Clockwise Routing” is proposed. The idea of the algorithm is that each router implements a simple digital automaton, which compares the distance between the current node and the destination node with the lengths of the descending formers, directing the packet to the corresponding port in the direction of maximum proximity to the destination node. In this way, each router makes a decision 1 step ahead, ensuring that the packet gradually approaches the destination node.

This algorithm is characterized by low hardware costs, but it is deterministic; i.e., it does not take into account many route variants and is not robust to network errors. In addition, it is proved in [2*] that it is not optimal (it is possible to have a shorter path along the global loop formed by a longer formant) (Figure 9).

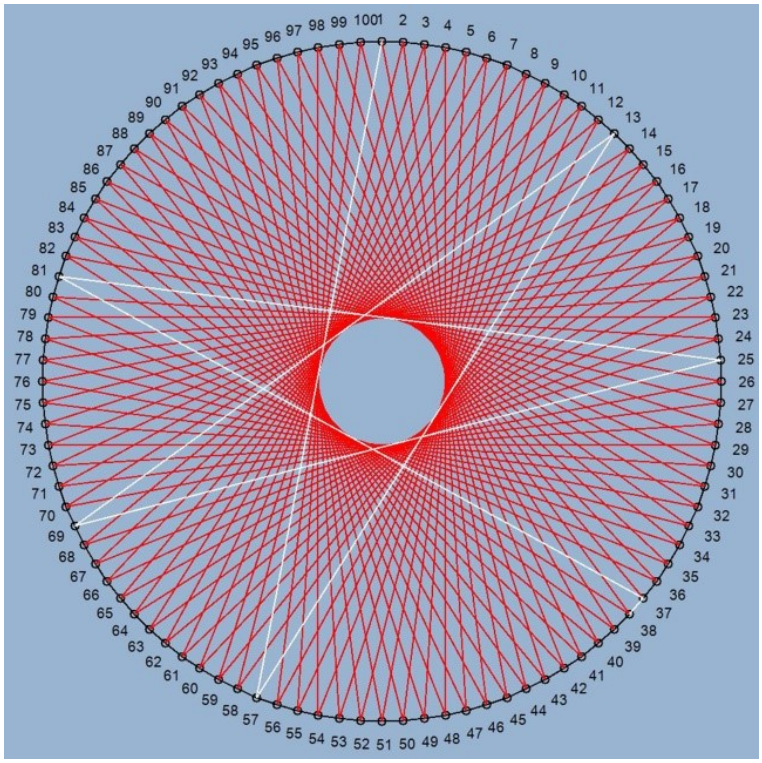


Figure 9 – Shortest path in the circulant $C(100;\ 1, 44)$ from node 1 to node 38 [2*].

An improved optimal version of this algorithm – “Adaptive Clockwise Routing” – requires significantly more resources [4*].

All the algorithms presented above were implemented for the case of two-dimensional circulants but can be easily transferred with improvements to other families of circulant graphs [5*]. Routing algorithms were also developed for specific families, such as $C(N;\ D;\ D+1)$ [121] (proposed in [81, 114]), multiplicative circulants [123–125], and three-dimensional ring circulants [5*] [126–130], which take into account the topological features of these families of graphs.

The peculiarity of the described algorithms is that they are developed on the basis of various heuristically developed rules by studying the peculiarities of certain families of circulant graphs using the principle of greedy advancement, when the choice of the next step is based on the principle of maximum proximity to the destination node. They are simple to implement and represent a balance between the cost of logic elements, memory blocks, and the value of the efficiency factor (the ratio of the sum of the length of all paths to the sum of the shortest paths in the graph). The developer can choose among the available routing algorithms the one that meets the requirements of the network-on-chip. Nevertheless, the fact that most of them are not optimal required the use of mathematical methods to develop new routing algorithms with guaranteed optimality.

An example of such an algorithm is the "Algorithm with calculation of the coefficients of the generatrices" described in [5*]. Its idea is that the path between two vertices of a three-dimensional circulant can be represented as a formula:

$$N \cdot c + dist = a_1 s_1 + a_2 s_2 + a_3 s_3,$$

where N – the number of vertices, c – the number of complete turns in the graph, $dist$ – the modulus of the difference between the vertex numbers, a_i – coefficient at s_i form.

The algorithm is to use the brute force method to select values a_1, a_2, a_3 and c such that $\sum_i |a_i| \to min$. The range of coefficient values for each circulant graph can be calculated in advance. In this case, the algorithm can be parallelized at the hardware level, and its complexity is $O(1)$.

Another routing algorithm found by using mathematical methods is the "Pairwise Exchange Algorithm"; it is described in [3*]. It is intended to be used in the popular family of optimal two-dimensional circulants of the form $C(N;\ D;\ D+1)$ [81, 114], since this is practically the only family of optimal circulant graphs that can be described by a formula. By applying the graph tessellation method in the plane (Figure 10), we formulated an algorithmic description of a routing algorithm having complexity $O(1)$ and proved its optimality.

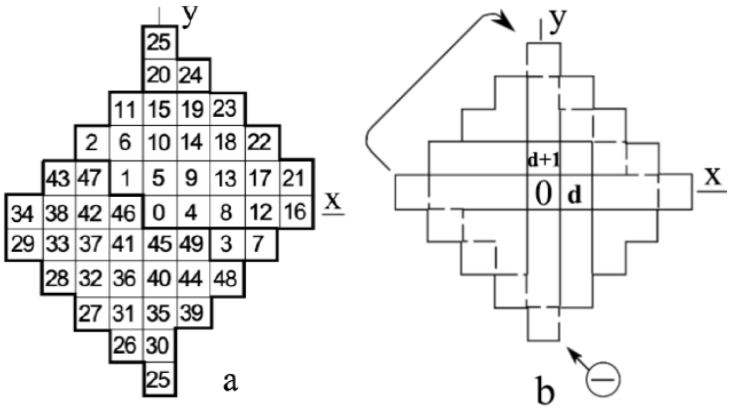


Figure 10 – Tessellation of graph $C(50;\ 4, 5)$ on the plane [3*]

It has lower hardware cost compared to the previous heuristics-based algorithm developed and has lower algorithmic complexity than algorithms derived and applied to this family of circulants by other scientists (Table 1).

Table 1 - Time complexity of routing algorithms for two-dimensional circulants

Algorithm	**Topology**	**Time complexity**	**Optimality**
Pairwise exchange algorithm [3*]	$C(N; D, D+1)$	$O(1)$	Yes
Robic [118]	$C(N; s_1, s_2)$	$O(N^{1/2})$	Yes
Dobravec et al. [119]	$C(N; s_1, s_2)$	$O(\log N)$	Yes
Zerovnik et al. [120]	$C(N; s_1, s_2)$	$O(\log N)$	Yes
Gomez et al. [121]	$C(N; s_1, s_2)$	$O(\log N)$	Yes
Chen et al. [122]	$C(N; s_1, s_2)$	$O(2 \log N)$	Yes
Martinez et al. [123]	$C(N_D; D, D+1)$	$O(D)$	Yes

Thus, the developed deterministic quasi-optimal and optimal single-step and multistep routing algorithms for different families of circulant graphs give the possibility of traffic routing in networks on-chip based on circulant topologies and provide the developer with the choice of the most suitable algorithm for the tasks of designing networks-on-chip. The described methodology of algorithm development on the basis of heuristic rules or by applying mathematical methods allows developing routing algorithms for circulant graphs with any parameters.

3.5 Adaptive routing algorithms

The use of deterministic routing algorithms in a network-on-chip is justified if it is known that it will function under conditions of low traffic load, or the loss of packets transmitted between nodes for computational tasks to be performed by the network-on-chip is acceptable. Another disadvantage of deterministic routing algorithms is that if a network is to experience such a phenomenon as “hot spots” (nodes that are most active compared to their neighbors in generating or consuming network traffic) [11*], it will lead to even greater network congestion, up to the inability to provide the necessary throughput.

If a more even distribution of traffic in the network is required, and if it is necessary to ensure that a packet can bypass busy parts of the network, adaptive routing algorithms are used.

For networks-on-chip of the form $C(N; D; D+1)$, in [6*], the ideas of the previously developed deterministic "Pairwise Exchange Algorithm" were developed [3*]. A fast procedure for calculating route vectors based on the geometric principle of neighborhoods (Figure 11) and a basic algorithm was proposed. These vectors - once calculated - are further stored not in all nodes of the network but only in the reference nodes (Figure 12) in the form of mapping tables.

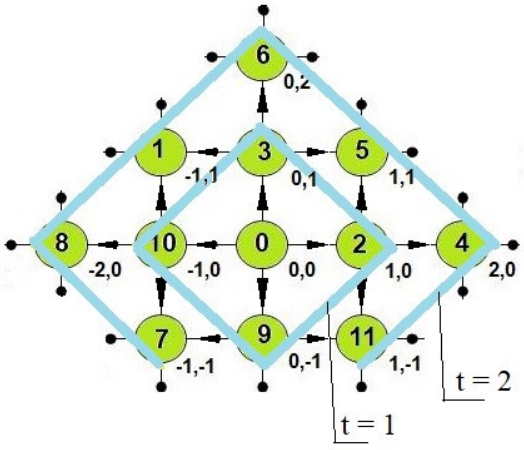


Figure 11 - Geometric principle of neighborhoods [6*] [137]

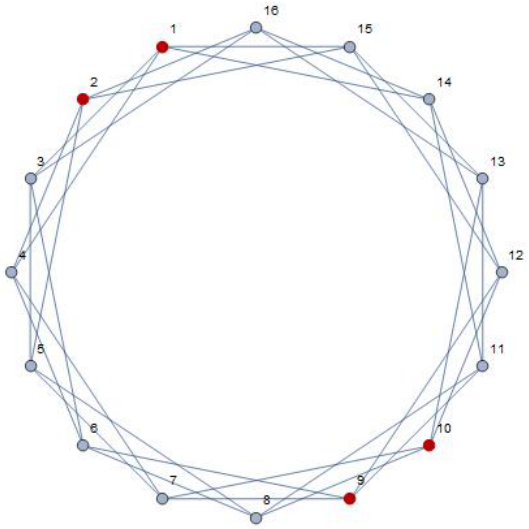


Figure 12 - Example of reference node arrangement in a network-on-chip [6*]

It was proved that (taking into account the symmetry of the circulant) it is sufficient to store route tables for only half of the nodes and half of the routes. It was also proposed to modify the routers so that they could exchange information about their workload with each other. Thus, the adaptability of the routing algorithm was ensured by selecting the next step, taking into account the information about the availability of neighboring nodes.

Adaptive routing algorithms improve load balancing in the network and speed up packet progression; they are robust to disruptive events such as flit blocking, router or link failures [41]. However, they are more complex and often require the use of resource-intensive operations (multiplication, division, modulo division, etc.) that are not always efficiently synthesized at the RTL layer.

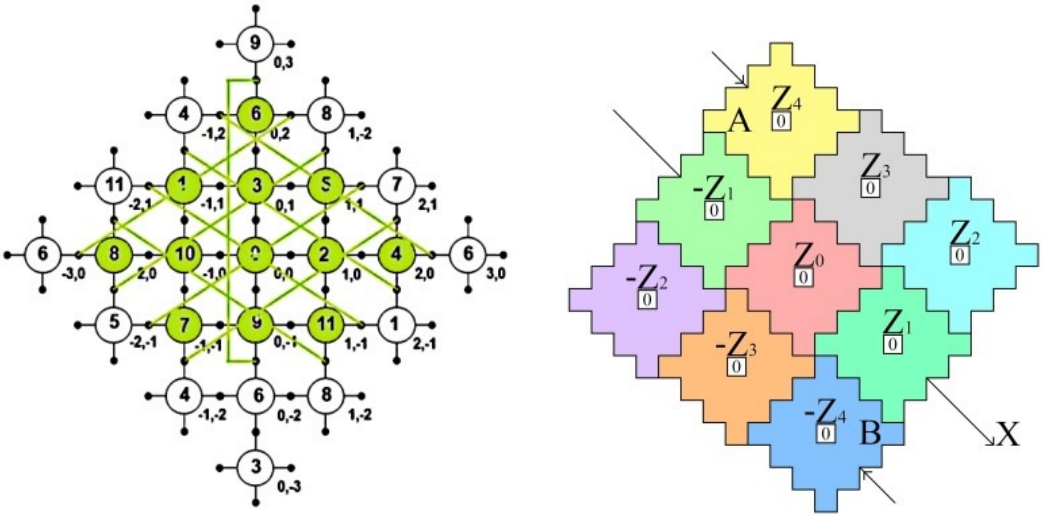
In [7*] two algorithms for the family of circulants are developed

$$C(N;\ s_1,\quad s_2) = \begin{cases} C(N;\ D-1,\quad D), & N_{D-1} < N \le 2D^2, \\ C(N;\ D,\quad D+1), & 2D^2 < N \le N_D, \end{cases}$$

where $N_D = 2D^2 + 2D + 1$ (GRBT algorithm) or $N = 2D^2 + D$ (SRBT algorithm).

Their peculiarity is that only basic arithmetic operations are used to compute the next step, and the complexity is $O(1)$. These algorithms also use the concept of reference nodes but in a different sense. These are the nodes with respect to which addressing is performed in the network. This means that the location and coordinates of the nodes in the network are determined not by their numbers (Figure 13a) but by the distances from the reference nodes.

Using the graph tessellation method in the plane (Figure 13b), the choice and location of reference nodes (as well as the unambiguity of addressing in such a network) are justified.



a) b)

Figure 13 – a) Graph representation $C(12;\ 2, 3)$ in the plane;
b) Tessellation of the graph $C(25;\ 3,\ 4)$ in the plane with marking of reference vertices [7*]

The essence of the GRBT algorithm is to select a zero reference vertex and other reference vertices symmetric to it with coordinates calculated by the proposed algorithm. To find the vector of the shortest paths from one vertex to another, we need to subtract their coordinates and compare the normalized length with the diameter. If it is larger than the diameter, then we should add the coordinates of the reference vertices to the obtained coordinates and take the final pair with the

minimum normalized length. Otherwise, this pair will be the desired path vector. Thus, the algorithm represents only arithmetic operations of addition and subtraction of coordinates without heavy weight operations of division and so on. The SRBT algorithm works on a similar principle but uses a smaller number of reference vertices, due to the fact that it is applicable to a much smaller set of circulant graphs.

Figure 14 shows the shortest path equal to $(-2, -1)$ calculated by the GRBT algorithm (red line) and alternative, longer paths (labeled in green) from vertex 6 $(-1, 2)$ (red asterisk) to the vertex 3 $(2, -1)$ (indicated in blue).

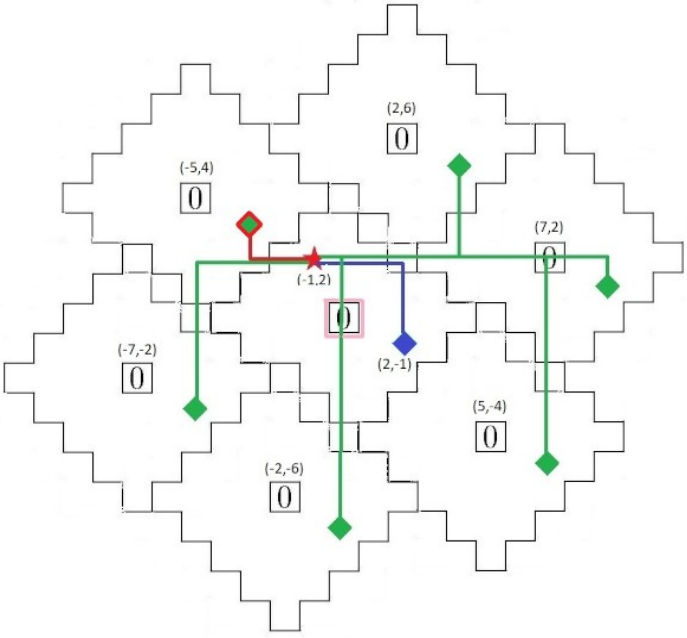


Figure 14 – Example of calculating possible paths to a destination node from the neighborhoods of neighboring reference nodes calculated by the GRBT algorithm [7*]

The adaptability of the proposed algorithms consists in the fact that they return a vector of paths, which consists of the number of transitions along the generators (in the considered example, there are 2 generators). If the number is negative, the transition is counterclockwise. The router can (based on the information about the load of neighboring routers or paths) choose the next hop to be made along the path.

Although both proposed algorithms are applicable for a limited set of circulants, they provide higher path computation speed for 32–56% of the routes (compared to the more universal analytical algorithm described previously [3*]), as well as commensurate resource costs.

Thus, by the example of developing algorithms from this section, the possibility of creating specialized algorithms for different families of circulant graphs is shown (taking into account their peculiarities and requirements to the implementation of these algorithms in hardware by using methods of graph tessellation in the plane, reference nodes, relative addressing, and so on).

3.6 Routing algorithm based on self-organization and relative addressing

The idea of using reference nodes and a coordinate system based on the distances from them was developed into a universal algorithm applicable to any topology [12*] [77, 110].

We proposed an algorithm for selecting reference nodes, which ensures their uniform placement in the network in a minimum sufficient number to ensure the desired network diameter. The reference nodes can be placed in advance or during the network operation, implementing the principle of self-organization borrowed from the field of wireless networks [138–141].

A virtual coordinate system representing the node address as a vector of distances from the reference nodes is justified [142]. Thus, addressing in the network is performed relative to the reference nodes and is unambiguous.

It is proposed to select the direction of package movement according to the following algorithm:

Let there be 4 reference nodes. We need to find the path from the node i with coordinates (A_i, B_i, C_i, D_i) to the node j with coordinates (A_j, B_j, C_j, D_j). The route can be characterized by the vector M_{ji} with coordinates $(A_j - A_i, B_j - B_i, C_j - C_i, D_j - D_i)$.

The direction of the packet movement is chosen to the neighboring node $k(i)$ for which the scalar product of vectors $M_{ji} * M_{ki}$ is maximized. That is, the will be selected that node $k(i)$ through which there is a maximum approach to the final node j.

The scalar product is defined in the standard way as the sum of products of corresponding coordinates of two vectors

$$M_{ji} \times M_{ki} = (A_j - A_i)(A_k - A_i) + (B_j - B_i)(B_k - B_i) +$$
$$+(C_j - C_i)(C_k - C_i) + (D_j - D_i)(D_k - D_i).$$

The proposed algorithm is quite simple to implement and does not depend on the topology structure. At the same time, it has a very useful property that allows using it in conditions of network errors: if one of the neighboring nodes (routers) of the network or its connection fails, it is excluded from calculations until its operability is restored. This means that the packet will be routed along the shortest path bypassing the failed nodes and connections (Figure 15).

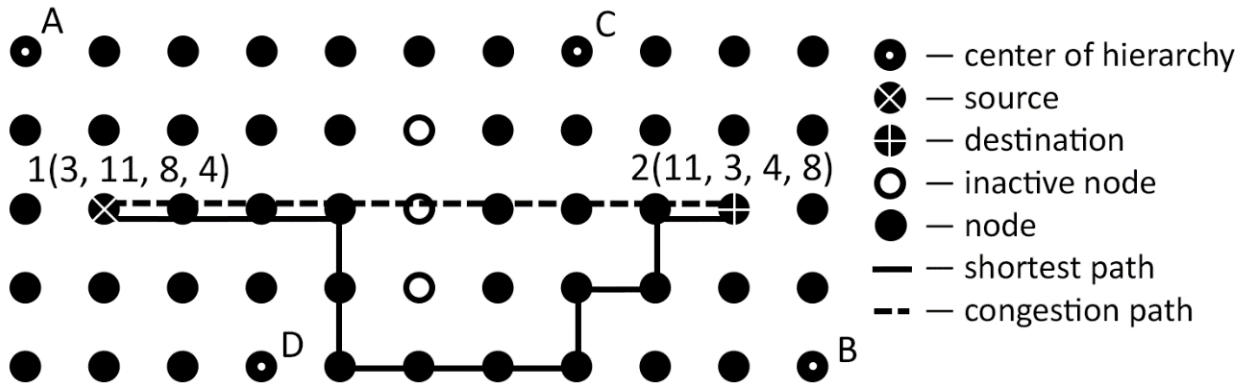


Figure 15 – Example of operation of the proposed routing algorithm when network errors occur [12*]

For the cases when the scalar products for two directions are equal, a set of rules is proposed in [12*], which allows solving the phenomenon of "starvation" of the network [143] – to avoid infinite returns $(167 \to 183 \to 167 \to \cdots)$ and loops $(166 \to 167 \to 183 \to 182 \to 166 \to \cdots)$ (Figure 16).

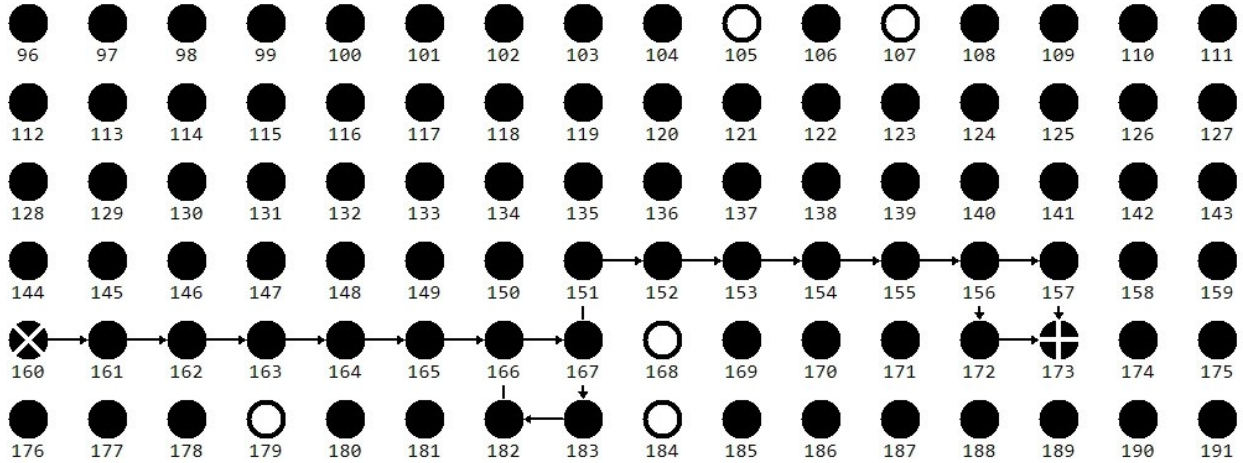


Figure 16 – Example of the operation of the proposed routing algorithm under infinite loops and returns [12*]

As a result of modeling and comparison with other known algorithms [144], which can deal with single errors in the network, the developed algorithm showed high adaptability and robustness to network errors (Figure 17).

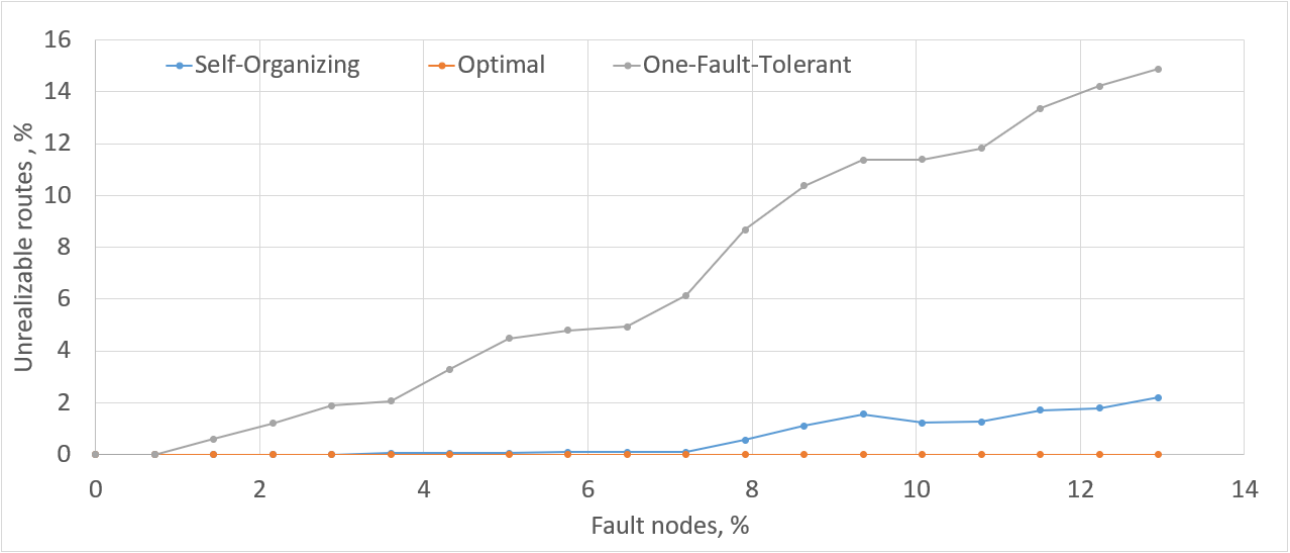


Figure 17 – Dependence of the number of unreachable routes on the number of failed nodes in the test network [12*]

3.7 A method for managing deadlock-free data transmission based on acyclic subnetwork

The phenomenon of node or link failure in a network is usually a sign of poorly chosen router architecture or network design errors. A more common and no less destructive phenomenon in networks on-chip are deadlocks [4, 41] – mutual blocking of packets due to cyclic dependencies, when data packets are waiting for each other. An example of such a cycle is shown in Figure 18.

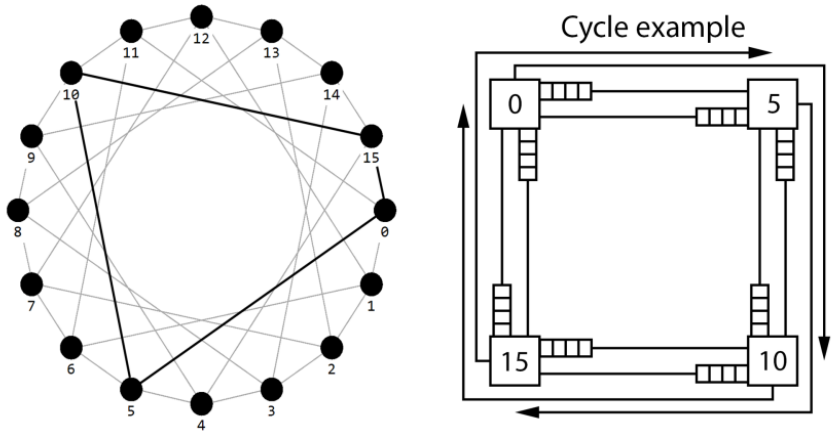


Figure 18 – Example of a loop in a circulant graph and illustration of mutual packet blocking in routers forming a loop [9*]

Deadlocks are combated at the level of traffic control by means of additional hardware redundancy and adjustments to routing algorithms. In [9*] an additional acyclic subnetwork [145] was proposed; with its help, a packet can bypass a blocked section in the network-on-chip. Here, hardware redundancy is added at the connection level [146]. The acyclic subnetwork is a tree of additional connections between nodes the root of which is the 0-th node; the tree itself covers all the nodes and has no cycles (an island tree) (Figure 19).

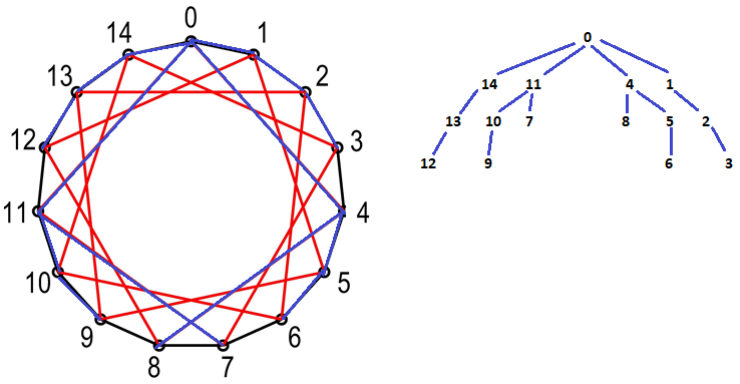


Figure 19 – Example of an acyclic tree for a circulant graph $C(15;\ 1, 4)$

If a deadlock occurs, the packet is moved to the acyclic subnet and continues to move through it, thus resolving cyclic dependencies in the network.

By means of high-level simulation and using the developed network-on-chip NewXim model [9*], it was demonstrated that when the threshold value is reached, the network throughput drops to the level of acyclic subnetwork throughput. It was also shown that using a tree with minimum Wiener index [147] provides better throughput of acyclic subnetwork (Figure 20).

Thus, due to a relatively small hardware redundancy, it is possible to get rid of the deadlock phenomenon, and there can be any basic routing algorithm. The disadvantage of this approach is that it is necessary to accurately plan the network load, because there is a danger of a sharp decrease in its capacity when the load threshold is exceeded.

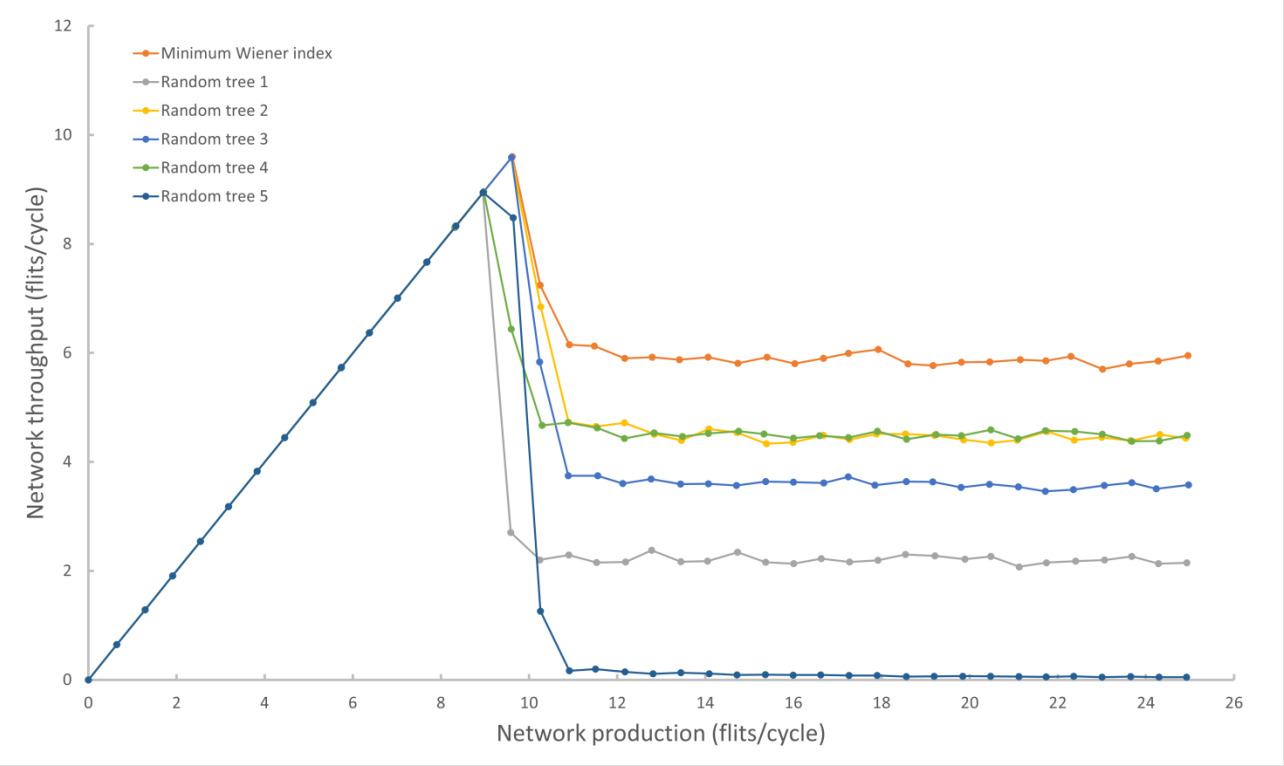
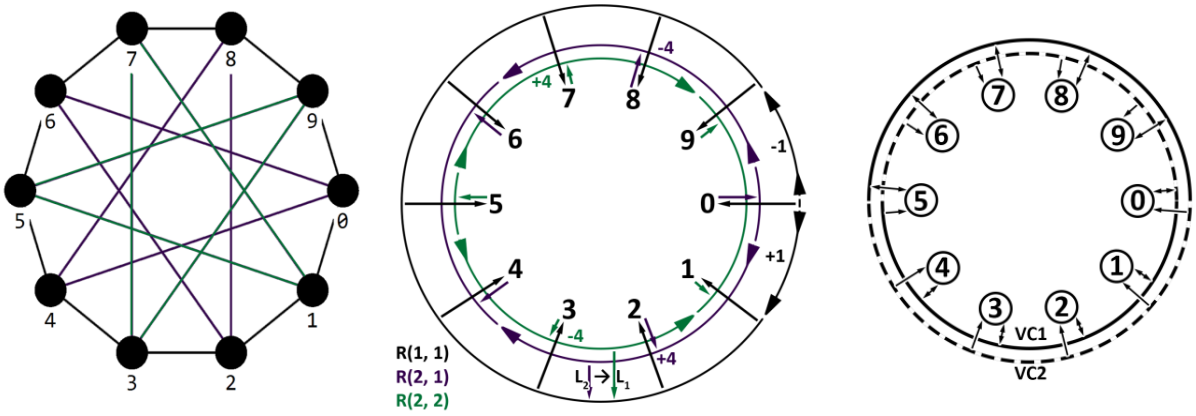


Figure 20 – Network throughput modeling results depending on the choice of reference graph type for acyclic subnetwork [9*]

3.8 Method for managing deadlock-free data transmission based on virtual channels and decomposition of the topology graph into subnets

For networks on-chip with mesh and torus topologies, the most popular and effective methods to combat deadlocks are based on the use of virtual channels [41, 148] and rules for changing packets in a network of virtual subnets (formed by virtual channels) in order to break cycles and eliminate the possibility of their occurrence. A virtual channel is the introduction of redundancy at the router level, where queues at its inputs are logically divided into multiple independent flows (Figure 7). Packets move through their virtual subnetwork formed by virtual channels and (according to certain rules) can change it so as not to block other packets.

In [9*] this approach was applied to the circulant topology. For this purpose, a method of splitting the topology graph into rings ("Ring–split") was developed [146]. A transition between rings means a change of virtual channel. Thus, several isolated looped logical routes are formed in the circulant graph. A packet which moves along them according to the developed rules moves from one ring to another and changes the virtual channel, which excludes the deadlock possibility (Figure 21a, b). In this case, the probability of cyclic blocking inside the ring tends to zero, since deadlocks (as a rule) are formed in cycles of no more than 4 transitions, and the formation of a deadlock to cover the entire ring is practically impossible. But to guarantee the complete absence of deadlocks, another rule is proposed: according to it, the ring is divided into semi-rings, and the transition between them also means the change of the virtual channel (Figure 21c).



a) b) c)

Figure 21 – Decomposition of a circulant graph $C(10;\ 1, 4)$ into subnets using Ring- split method to fight deadlocks [9*]

Using high-level modeling, it was shown that the proposed approach is universal and can be implemented for any method of organizing queues in the routers: queues can be either large to accommodate the entire packet (store-and-forward [4]), or reduced in size, accommodating only a

few flits of a packet stretching across the network (wormhole [41]). Breaking cyclic dependencies in both cases avoids deadlocks.

Comparative modeling of the developed data transmission control method showed that it does not have the problem of a sharp decrease in throughput as with the method using an acyclic subnet. Both methods work with any routing algorithm, so the “Paired Exchange Algorithm” [3*] (developed earlier) was taken for routing. It was shown that using a new method of traffic management in a network-on-chip with a circulant topology allows one to achieve significantly higher throughput than in a network-on-chip with the same number of nodes but with a mesh topology and an XY routing algorithm using virtual channels. An example of simulation results in the NewXim simulator of various variants of networks-on-chip with 64 nodes is shown in Figure 22.

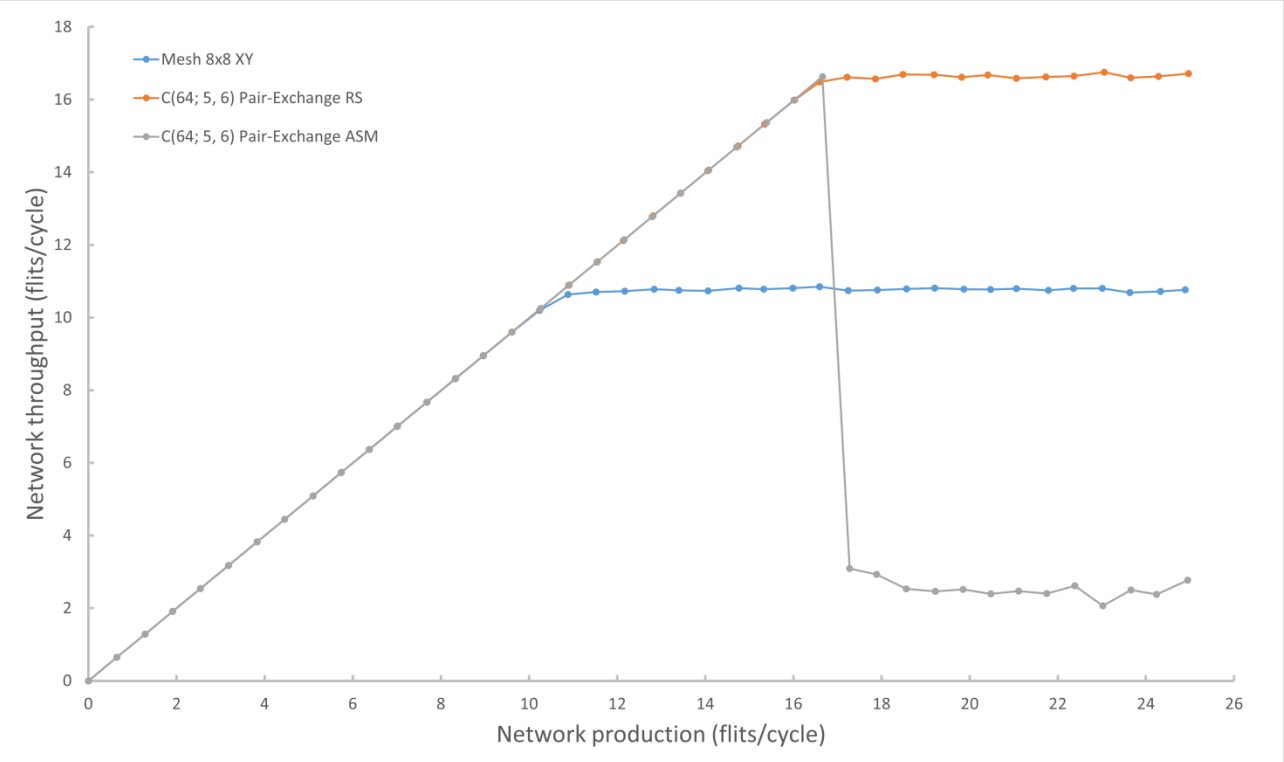


Figure 22 – Comparison of traffic control methods in networks-on-chip with circulant topology (acyclic subnet and Ring-split / virtual channels) and with mesh topology (XY / virtual channels) [9*]

3.9 Decomposition methods for circulant graphs

Decomposition of a circulant graph into subgraphs in which there are no cycles combined with the principle of separating traffic flows using virtual channels (as shown in [9*]) makes it possible to effectively combat the deadlock phenomenon. But this method requires introducing quite significant redundancy into routers, which must take into account the history of the packet’s movement and the intersection of the boundaries of rings and semi-rings along its path.

At the same time, mathematicians have been studying the decomposition of circulant graphs for a long time. Basically, these works are carried out in two directions: decomposition of the circulant into cycles [149–152] and decomposition into simpler graphs [152–154]. The first group of methods is suitable for implementing the Ring-split approach described earlier; the second group opens up the possibility of using the virtual channel method to combat deadlocks by analogy with Ring-split but changing the channel when a packet moves from one subgraph to another.

Using the example of decomposition of bipartite circulant graphs based on Cartesian and tensor products, it is shown in [10*] that if the subgraphs into which the decomposition is performed are acyclic, then it is possible to implement deadlock-free routing based on the rule of changing the virtual channel when moving from one subgraph to another (Figure 23).

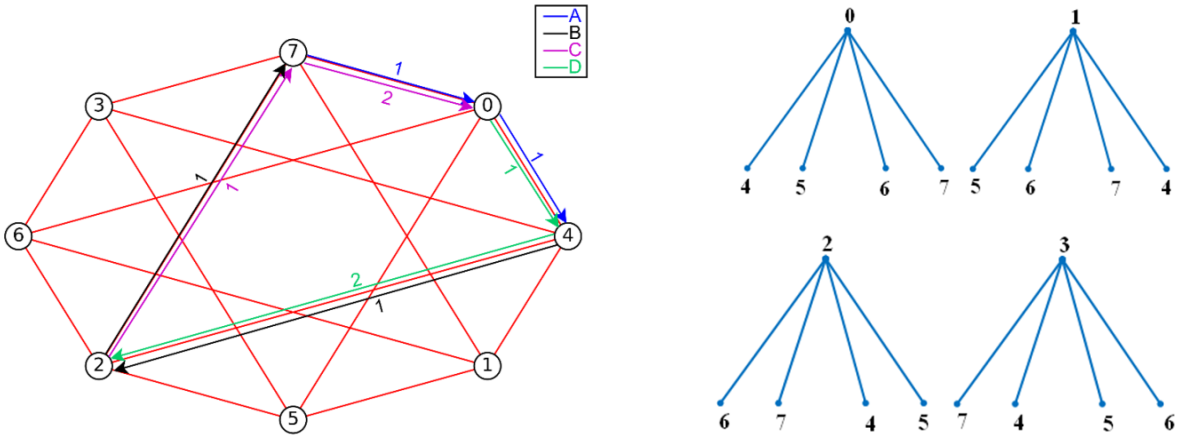


Figure 23 – Breaking the cyclic dependency between nodes $0-4-2-7$ in a graph $C(8;\ 1,3)$ by decomposing it into subgraphs $K_{1,4}$ and using the virtual channels [10*]

Decomposition of circulant graphs can also be used to optimize the network structure and reduce hardware costs. Thus, in [152] it was proposed to perform segmentation of strongly connected large-order circulant graphs into caterpillar subgraphs (Figure 24).

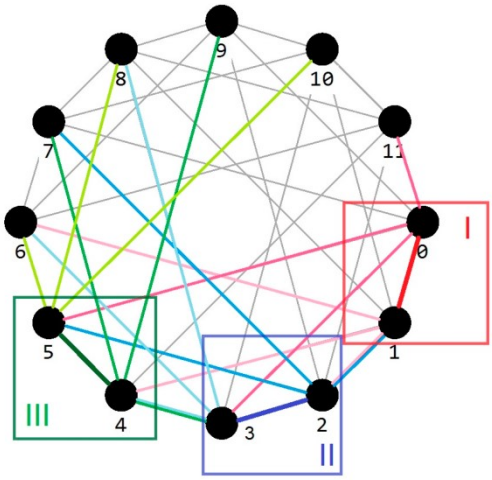


Figure 24 – Segmentation of the graph $C(12;\ 1,3,5)$ into caterpillar subgraphs $C_2(3,3)$. I, II, III – network segments [152]

The peculiarity of caterpillar graphs is that they have a skeleton that forms a path and branches of unit length. It is proposed to implement the principle of locality; according to it, in most applications, the most intensive exchange is carried out between neighboring nodes that are spatially located nearby. This means that the backbone of the caterpillar graph can be implemented by a connection with a higher throughput, and the branches – with a smaller one. It is also proposed to implement a hierarchical network organization based on the principle of classical communication networks, when individual segments in a common network can have global addresses, and nodes in the segment can have local addresses, as well as a common routing table. This makes it possible to reduce hardware costs and increase network throughput, as well as eliminate the problem of deadlocks, due to the fact that individual network segments are acyclic, and the formation of a cycle of several segments is unlikely because of the different throughput of connections inside and outside the segments and the distribution of traffic in them.

4 Conclusions

The dissertation presents a new, developed by the author approach to the design of networks-on-chip, which is based on the use of circulant topologies as the topology of the communication subsystem of networks-on-chip. To implement it in the practice of designing networks-on-chip, new methods for synthesizing optimal circulant graphs, new high-level and low-level models, as well as tools for prototyping networks-on-chip were developed, support for circulant topologies, new single-step and multi-step deterministic routing algorithms, adaptive routing algorithms, new methods for dealing with errors in the network, new methods for managing traffic in networks-on-chip, allowing to eliminate the problem of deadlocks (arising due to the peculiarities of circulant topologies), as well as methods for segmenting circulant graphs for their use in networks-on-chip were added. The author clearly demonstrates the advantages of circulant topologies over the classical mesh and torus topologies.

The new results presented in this thesis are important both for further theoretical research on the design of networks-on-chip and for the creation and development of new automated tools for their design.

Twelve articles submitted by the author for protection of the dissertation contain 144 journal pages; these works co-authored with the leading scientists and published in peer-reviewed journals were indexed in the scientific citation databases Scopus and WoS (10 of them – in journals with Q1, Q2 quartiles).

The following new results summarized above, rigorously mathematically proven or validated by simulation and prototyping in relevant published articles are presented for protection:

1. A new approach to designing networks-on-chip based on circulant topologies.

   The statement about the possibility of applying this approach in practice and its advantages over other approaches (using other topologies) is based on the results described below. The author not only proposed a new approach but also carried out its comprehensive study; as a result, circulant graphs with the required parameters were obtained and their characteristics were assessed; a methodology for studying networks-on-chip with new topologies was developed for which the necessary tools at different levels of abstraction were created; routing methods in networks-on-chip based on circulant topologies were proposed, and a number of different routing algorithms built on different principles and ensuring a balance between performance and resource intensity were developed; traffic control methods were proposed that allow (at the level of the routing algorithm) combatting such destructive phenomena as failure of elements of the communication subsystem and mutual blocking of packets.

2. An algorithm for calculating the shortest paths in a circulant graph and methods for speeding up the procedure for enumerating graph signatures to synthesize new circulant graphs.

   On their basis, a calculation scheme in the form of software was developed and implemented, where the procedure for searching for optimal circulant topologies was accelerated up to 35,000 times compared to exhaustive methods, which made it possible to synthesize the necessary sets of graphs with order and dimension covering all current and future needs for using circulant graphs as topologies for designing networks-on-chip.

3. Dataset of optimal circulant graphs with order up to 1000 and dimension up to 10.

   The presented dataset (the first of its kind) is a reference for the development of new datasets in this area. It allows exploring circulant graphs more deeply, identifying regular dependencies between graph characteristics, training machine learning models to predict graph characteristics, searching for new families of circulant graphs, and solving other problems. The dataset is used by a number of independent scientists to test the performance of their algorithms used to synthesize optimal circulant graphs.

   It is shown that it makes sense to search for optimal circulant graphs for problems of application in networks-on-chip among a subset of ring circulants, which makes it possible to reduce by 1 the number of degrees of freedom of the search procedure.

4. New and modified models of different levels of abstraction and tools for prototyping networks-on-chip that support circulant topologies.

   A generalized ECAD architecture that provides a unified route for designing networks-on-chip implementing the principle of end-to-end design is proposed. For the main stages of network-on-chip modeling and prototyping, new models of networks-on-chip of different levels of abstraction were developed and existing models of networks-on-chip were adapted; tools for prototyping networks-on-chip were created and unified formats for data transfer between different stages of designing networks-on-chip were described. Their main advantage over existing tools is that they are combined within a single design route and support the circulant topology, which made it possible to conduct a comparative analysis of the results of modeling circulant and other network-on-chip topologies, as well as the implementation of various routing algorithms to fight deadlocks and network errors, which confirmed the advantages of the new solutions proposed.

5. Deterministic routing algorithms for networks-on-chip based on different families of circulant topologies.

   A whole family of different deterministic routing algorithms suitable for any circulant were developed ("Clockwise Routing", "Adaptive Clockwise Routing", "Algorithm with calculation of constituent coefficients"). Routing algorithms that take into account topological features of specific graph families were also proposed (multiplicative circulants, $\mathrm{C}(N;\ D;\ D+1)$ (including the "Pairwise Exchange Algorithm"), three-dimensional ring circulants, and others). The developed algorithms differ among themselves in resource consumption and efficiency; they can be single-step and multi-step, which allows choosing a suitable algorithm for a particular design problem.

6. Adaptive routing algorithms for networks-on-chip based on different families of circulant topologies.

   Based on the deterministic "Pairwise Exchange Algorithm", its adaptive version is developed, which allows the router to choose the next step based on the information about the load or availability of neighboring nodes, which leads to better load balancing in the network and faster packet progression and increases the robustness against destructive phenomena (packet blocking, failure of routers or links).

   In order to partially offset the disadvantage of adaptive algorithms consisting in higher resource consumption compared to simpler deterministic algorithms two (GRBT, SRBT)

adaptive algorithms (implemented only on arithmetic operations, most efficiently realized at the transistor level) are developed for a limited family of circulants.

7. A routing algorithm based on self-organization and relative addressing for routing traffic in networks-on-chip based on circulant topologies in conditions of failure of individual network nodes or connections.

   A universal high-level routing algorithm, which incorporates the ideas of other algorithms, as well as routing principles used in classical communication networks is proposed. It consists of marking support nodes (the principle of self-organization) evenly distributed in the network in a minimum quantity sufficient to ensure the required network diameter. The reference nodes form a virtual coordinate system based on the distances from them (relative addressing principle). The node address (as well as the direction of movement of the packet to the destination node) in such a coordinate system is represented as a vector of distances from the reference nodes and is unambiguous. In this case, routing is carried out by calculating scalar products between the direction vector of movement and the addresses of neighboring nodes. This makes the algorithm universal and independent of the topology and changes in the network configuration, which determines its resistance to failure of individual network nodes or connections.

8. Control methods for deadlock-free data transmission in networks-on-chip with circulant topologies.

   A method to combat deadlocks in a network-on-a-chip with a circulant topology, based on the use of an acyclic subnetwork, which provides guaranteed throughput at the level of this subnetwork when the communication subsystem is overloaded was developed. It is shown that the use of an acyclic tree with a minimum Wiener index provides the best throughput of an acyclic subnet.

   A method for managing deadlock-free data transmission in networks-on-chip with circulant topologies based on the use of virtual channels and decomposition of the topology graph into acyclic subgraphs was developed. A method for decomposing circulant graphs into open rings, which guarantees the absence of deadlocks was developed. It is also shown that the proposed method of dealing with deadlocks is applicable to other methods of decomposition of circulant graphs using the example of decomposition of bipartite circulant graphs based on Cartesian and tensor products, as well as by segmenting circulant graphs into caterpillar subgraphs.

References

1. Jantsch A., Tenhunen H. Networks on Chip // Networks on Chip. MA: Springer US, 2003. 312 p. DOI: 10.1007/b105353.

2. Benini L., De Micheli G. Networks on chips: a new SoC paradigm // Computer (Long. Beach. Calif). 2002. Vol. 35, No. 1. P. 70–78. DOI: 10.1109/2.976921.

3. Kundu S., Chattopadhyay S. Network-on-Chip: The Next Generation of System-on-Chip Integration // Network-on-Chip. CRC Press, 2018. DOI: 10.1201/9781315216072.

4. Jerger N.E., Krishna T., Peh L.S. On-Chip Networks: Second Edition. Morgan and Claypool Publishers, 2017. 212 p. DOI: 10.2200/S00772ED1V01Y201704CAC040.

5. Marculescu R., Bogdan P. The Chip Is the Network: Toward a Science of Network-on-Chip Design // Found. Trends Electron. Des. Autom. 2007. Vol. 2, No. 4. P. 371–461. DOI: 10.1561/1000000011.

6. Bhanu P.V. et al. Fault-Tolerant Application-Specific Topology-Based NoC and Its Prototype on an FPGA // IEEE Access. 2021. Vol. 9. P. 76759–76779. DOI: 10.1109/ACCESS.2021.3082852.

7. Wolkotte P.T. et al. Energy Model of Networks-on-Chip and a Bus // 2005 International Symposium on System-on-Chip. IEEE, 2005. P. 82–85. DOI: 10.1109/ISSOC.2005.1595650.

8. Jayshree S.G., Pati D. Design and Area Performance Energy Consumption Comparison of Secured Network-on-Chip with PTP and Bus Interconnections // J. Inst. Eng. Ser. B. Springer, 2022. Vol. 103, No. 5. P. 1479–1491. DOI: 10.1007/s40031-022-00735-5.

9. Abbaszadeh M. et al. ANDRESTA: An Automated NoC-Based Design Flow for Real-Time Streaming Applications // Proc. RTEST 2020 – 3rd CSI/CPSSI Int. Symp. Real-Time Embed. Syst. Technol. IEEE, 2020. P. 1–8. DOI: 10.1109/RTEST49666.2020.9140136.

10. De Micheli G., Benini L. Networks on Chips: 15 Years Later // Computer (Long. Beach. Calif). IEEE, 2017. Vol. 50, No. 5. P. 10–11. DOI: 10.1109/MC.2017.140.

11. Das M.S. Architecture of Multi-Processor Systems using Networks on Chip (NoC): An Overview // CVR J. Sci. Technol. 2022. Vol. 22, No. 1. P. 7–15. DOI: 10.32377/cvrjst2202.

12. Chandrachoodan N. Network-on-chip basics. NPTEL-NOC IITM, 2019. P. 20. https://www.youtube.com/watch?app=desktop&v=7-KJ3BnFsr8.

13. Howser G. The OSI Seven Layer Model // Computer Networks and the Internet. Cham: Springer International Publishing, 2020. P. 7–32. DOI: 10.1007/978-3-030-34496-2_2.

14. Bjerregaard T., Mahadevan S. A survey of research and practices of Network-on-chip // ACM Comput. Surv. 2006. Vol. 38, No. 1. P. 1–es. DOI: 10.1145/1132952.1132953.

15. Lezhnev E. V. et al. Electronic Computer-Aided Design for Low-Level Modeling of Networks-on-Chip // IEEE Access. 2024. Vol. 12. P. 48750–48763. DOI: 10.1109/ACCESS.2024.3382710.

16. Deng Y. et al. Optimal low-latency network topologies for cluster performance enhancement // J. Supercomput. 2020. Vol. 76, No. 12. P. 9558–9584. DOI: 10.1007/s11227-020-03216-y.

17. Huang X., F. Ramos A., Deng Y. Optimal circulant graphs as low-latency network topologies // J. Supercomput. Springer, 2022. Vol. 78, No. 11. P. 13491–13510. DOI: 10.1007/S11227-022-04396-5.

18. Horro M. et al. Effect of Distributed Directories in Mesh Interconnects // Proceedings of the 56th Annual Design Automation Conference 2019. NY, USA: ACM, 2019. P. 1–6. DOI: 10.1145/3316781.3317808.

19. Dai M. et al. Don't Mesh Around: Side-Channel Attacks and Mitigations on Mesh Interconnects // Proc. 31st USENIX Secur. Symp. Secur. 2022. P. 2857–2874.

20. Ditzel D. et al. Accelerating ML Recommendation with over a Thousand RISC-V/Tensor Processors on Esperanto's ET-SoC-1 Chip // 2021 IEEE Hot Chips 33 Symposium (HCS). IEEE, 2021. P. 1–23. DOI: 10.1109/HCS52781.2021.9566904.

21. Paccagnella R., Luo L., Fletcher C.W. Lord of the Ring(s): Side Channel Attacks on the CPU On-Chip Ring Interconnect Are Practical // Proc. 30th USENIX Secur. Symp. 2021. P. 645–662. DOI: 10.48550/arXiv.2103.03443.

22. Papazian I.E. New 3rd Gen Intel ® Xeon ® Scalable Processor (Codename: Ice Lake-SP) // 2020 IEEE Hot Chips 32 Symposium (HCS). IEEE, 2020. P. 1–22. DOI: 10.1109/HCS49909.2020.9220434.

23. Chethan Kumar H.B. et al. 120-core microAptiv MIPS overlay for the Terasic DE5-NET FPGA board // FPGA 2017 – Proc. 2017 ACM/SIGDA Int. Symp. Field-Programmable Gate Arrays. Association for Computing Machinery, Inc, 2017. P. 141–146. DOI: 10.1145/3020078.3021751.

24. Grani P. et al. Design and Evaluation of AWGR-Based Photonic NoC Architectures for 2.5D Integrated High Performance Computing Systems // 2017 IEEE International Symposium on High Performance Computer Architecture (HPCA). IEEE, 2017. P. 289–300. DOI: 10.1109/HPCA.2017.17.

25. Lee D. et al. Performance and Thermal Tradeoffs for Energy-Efficient Monolithic 3D Network-on-Chip // ACM Trans. Des. Autom. Electron. Syst. 2018. Vol. 23, No. 5. P. 1–25. DOI: 10.1145/3223046.

26. Sun C., Ouyang Y., Lu Y. DCBuf: a high-performance wireless network-on-chip architecture with distributed wireless interconnects and centralized buffer sharing // Wirel. Networks. 2022. Vol. 28, No. 2. P. 505–520. DOI: 10.1007/s11276-021-02882-x.

27. Yahya M.R. et al. Optical Versus Electrical: Performance Evaluation of Network-on-Chip Topologies for UWASN Manycore Processors // Wirel. Pers. Commun. 2021. Vol. 116, No. 2. P. 963–991. DOI: 10.1007/s11277-019-06630-5.

28. Romanov A.Y., Amerikanov A.A., Lezhnev E.V. Analysis of Approaches for Synthesis of Networks-on-chip by Using Circulant Topologies // J. Phys. Conf. Ser. IOP Publishing, 2018. Vol. 1050, No. 1. P. 1–12. DOI: 10.1088/1742-6596/1050/1/012071.

29. Alimi I. et al. Network-on-Chip Topologies: Potentials, Technical Challenges, Recent Advances and Research Direction // Network-on-Chip - Architecture, Optimization, and Design Explorations. IntechOpen, 2022. DOI: 10.5772/intechopen.97262.

30. Bhowmik B. Dugdugi: An Optimal Fault Addressing Scheme for Octagon-Like On-Chip Communication Networks // IEEE Trans. Very Large Scale Integr. Syst. 2021. Vol. 29, No. 5. P. 1009–1021. DOI: 10.1109/TVLSI.2021.3059662.

31. Tatas K. et al. The Spidergon STNoC // Designing 2D and 3D Network-on-Chip Architectures. NY: Springer New York, 2014. P. 161–190. DOI: 10.1007/978-1-4614-4274-5_7.

32. Pai K.-J. et al. Configuring Protection Routing via Completely Independent Spanning Trees in Dense Gaussian On-Chip Networks // IEEE Trans. Netw. Sci. Eng. 2022. Vol. 9, No. 2. P. 932–946. DOI: 10.1109/tnse.2022.3140329.

33. Bhanu P.V., Kulkarni P.V., Soumya J. Butterfly-Fat-Tree topology based fault-tolerant Network-on-Chip design using particle swarm optimisation // J. Exp. Theor. Artif. Intell. 2019. Vol. 31, No. 5. P. 781–799. DOI: 10.1080/0952813X.2019.1597174.

34. Zhang H., Wang X. KGT: An Application Mapping Algorithm Based on Kernighan–Lin Partition and Genetic Algorithm for WK-Recursive NoC Architecture // Lect. Notes Comput. Sci. (Including Subser. Lect. Notes Artif. Intell. Lect. Notes Bioinformatics). 2021. Vol. 12836 LNCS. P. 86–101. DOI: 10.1007/978-3-030-84522-3_7.

35. Rzaev E., Ryzhov A., Romanov A. The New Promising Network-on-Chip Topologies Development Using Hierarchical Method // 2022 International Conference on Industrial Engineering, Applications and Manufacturing (ICIEAM). IEEE, 2022. P. 819–824. DOI: 10.1109/ICIEAM54945.2022.9787143.

36. Ali M.N.M. et al. SCCN: A Time-Effective Hierarchical Interconnection Network for Network-On-Chip // Mob. Networks Appl. Mobile Networks and Applications, 2019. Vol. 24, No. 4. P. 1255–1264. DOI: 10.1007/s11036-019-01262-2.

37. Liu H., Li X., Wang S. Construction of Dual Optimal Bidirectional Double-Loop Networks for Optimal Routing // Mathematics. 2022. Vol. 10, No. 21. P. 4016. DOI: 10.3390/math10214016.

38. Meng Y. et al. Graph Similarity-Based Maximum Stable Subgraph Extraction of Information Topology from a Vehicular Network // IEEE Trans. Intell. Transp. Syst. 2022. Vol. 23, No. 1. P. 355–367. DOI: 10.1109/TITS.2020.3011100.

39. Khan S. et al. Comparative analysis of network-on-chip simulation tools // IET Comput. Digit. Tech. Wiley Online Library, 2018. Vol. 12, No. 1. P. 30–38.

40. Ben A., Ben S. A Survey of Network-On-Chip Tools // Int. J. Adv. Comput. Sci. Appl. 2013. Vol. 4, No. 9. DOI: 10.14569/IJACSA.2013.040910.

41. Benmessaoud Gabis A., Koudil M. NoC routing protocols – objective-based classification // J. Syst. Archit. Elsevier B.V., 2016. Vol. 66–67. P. 14–32. DOI: 10.1016/j.sysarc.2016.04.011.

42. Khare A., Patil C., Chattopadhyay S. Task mapping and flow priority assignment of real-time industrial applications for network-on-chip based design // Microprocess. Microsyst. Elsevier, 2020. Vol. 77. P. 103175. DOI: 10.1016/J.MICPRO.2020.103175.

43. Wang C. et al. Dynamic application allocation with resource balancing on NoC based many-core embedded systems // J. Syst. Archit. Elsevier B.V., 2017. Vol. 79. P. 59–72. DOI: 10.1016/j.sysarc.2017.07.004.

44. Baby N. et al. Network on chip simulator: Design, implementation and comparison of Mesh, Torus and RiCoBiT topologies // 2nd International Conference on Next Generation Computing Technologies, NGCT 2016. 2017. P. 46–50. DOI: 10.1109/NGCT.2016.7877388.

45. Sai Kumar A., Hanumantha Rao T.V.K. An Efficient Low Latency Router Architecture for Mesh-Based NoC // Adv. Commun. Signal Process. VLSI. Lect. Notes Electr. Eng. Springer, 2021. Vol. 722. P. 241–248. DOI: 10.1007/978-981-33-4058-9_21.

46. Huang J. et al. Lagrangian relaxation-based routing path allocation for application-specific network-on-chips // Integration. Elsevier B.V., 2018. Vol. 61, No. June. P. 20–28. DOI: 10.1016/j.vlsi.2017.10.011.

47. Hojabr R. et al. Customizing Clos Network-on-Chip for Neural Networks // IEEE Trans. Comput. IEEE Computer Society, 2017. Vol. 66, No. 11. P. 1865–1877. DOI: 10.1109/TC.2017.2715158.

48. Kim J. et al. Technology-Driven, Highly-Scalable Dragonfly Topology // ACM SIGARCH Comput. Archit. News. 2008. Vol. 36, No. 3. P. 77–88. DOI: 10.1145/1394608.1382129.

49. Kim J., Balfour J., Dally W.J. Flattened butterfly topology for on-chip networks // IEEE Comput. Archit. Lett. IEEE, 2007. Vol. 6, No. 2. P. 37–40. DOI: 10.1109/L-CA.2007.10.

50. Jamali M.A.J. et al. A study on WK-recursive topology using gpNoCsim++ simulator and comparison to Other topologies // Proceedings – 17th IFIP International Conference on Very Large Scale Integration, VLSI-SoC 2009. IEEE Computer Society, 2009. P. 181–184. DOI: 10.1109/VLSISOC.2009.6041351.

51. Awal M.R., Rahman M.M.H., Akhand M.A.H. A new hierarchical interconnection network for future generation parallel computer // 16th Int'l Conf. Computer and Information Technology, ICCIT 2013. IEEE, 2014. P. 314–319. DOI: 10.1109/ICCITechn.2014.6997341.

52. Ali M.N.M. et al. The Static Performance Effect of Hybrid- Hierarchical Interconnection by Shifted Completely Connected Network // IEEE Access. IEEE, 2021. Vol. 9. P. 99249–99265. DOI: 10.1109/ACCESS.2021.3095146.

53. Manevich R. et al. Designing single-cycle long links in hierarchical NoCs // Microprocess. Microsyst. 2014. DOI: 10.1016/j.micpro.2014.05.005.

54. Montserrat J.S. NoC Topology synthesis using Metaheuristics. Universitat Politecnica de Catalunya, 2020. 87 p.

55. Mirka M. et al. GANNoC: A Framework for Automatic Generation of NoC Topologies using Generative Adversarial Networks // Proceedings of the 2021 Drone Systems Engineering and Rapid Simulation and Performance Evaluation: Methods and Tools Proceedings. NY, USA: ACM, 2021. P. 51–58. DOI: 10.1145/3444950.3447283.

56. Liu Zheng et al. Application-aware generation and optimization for NoC topology // 2009 IEEE Youth Conference on Information, Computing and Telecommunication. IEEE, 2009. P. 259–262. DOI: 10.1109/YCICT.2009.5382375.

57. Li Y. et al. A joint optimization method for NoC topology generation // J. Supercomput. 2018. Vol. 74, No. 7. P. 2916–2934. DOI: 10.1007/s11227-018-2339-0.

58. Narayanasamy P., Gopalakrishnan S., Muthurathinam S. Custom NoC topology generation using Discrete Antlion Trapping Mechanism // Integration. 2021. Vol. 76. P. 76–86. DOI: 10.1016/j.vlsi.2020.09.001.

59. Coppola M. et al. Spidergon: a novel on-chip communication network // 2004 International Symposium on System-on-Chip. IEEE, 2004. P. 15. DOI: 10.1109/ISSOC.2004.1411133.

60. Tatas K. et al. Designing 2D and 3D Network-on-Chip Architectures. NY: Springer New York, 2014. DOI: 10.1007/978-1-4614-4274-5.

61. Bhowmik B., Deka J.K., Biswas S. Improving Reliability in Spidergon Network on Chip-Microprocessors // 2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS). IEEE, 2020. P. 474–477. DOI: 10.1109/MWSCAS48704.2020.9184540.

62. Monakhova E.A. A Survey on Undirected Circulant Graphs // Discret. Math. Algorithms Appl. World Scientific Publishing Company, 2012. Vol. 4, No. 1. P. 1250002. DOI: 10.1142/S1793830912500024.

63. Elspas B., Turner J. Graphs with circulant adjacency matrices // J. Comb. Theory. 1970. DOI: 10.1016/S0021-9800(70)80068-0.

64. Beivide R. et al. Chordal topologies for interconnection networks // Lect. Notes Comput. Sci. (Including Subser. Lect. Notes Artif. Intell. Lect. Notes Bioinformatics). 2003. Vol. 2858. P. 385–392. DOI: 10.1007/978-3-540-39707-6_33.

65. Dharmasena H.P., Yan X. An optimal fault-tolerant routing algorithm for weighted bidirectional double-loop networks // IEEE Trans. Parallel Distrib. Syst. IEEE, 2005. Vol. 16, No. 9. P. 841–852. DOI: 10.1109/TPDS.2005.103.

66. Bermond J.C., Comellas F., Hsu D.F. Distributed loop computer-networks: A survey // J. Parallel Distrib. Comput. 1995. Vol. 24, No. 1. P. 2–10. DOI: 10.1006/jpdc.1995.1002.

67. Mukherjee A., Deb P.K., Misra S. Timed Loops for Distributed Storage in Wireless Networks // IEEE Trans. Parallel Distrib. Syst. IEEE, 2022. Vol. 33, No. 3. P. 698–709. DOI: 10.1109/TPDS.2021.3100780.

68. Liang C.H. et al. Performance evaluation of multi-exaflops machines using Equality network topology // J. Supercomput. 2023. Vol. 79. P. 8729–8753. DOI: 10.1007/s11227-022-05005-1.

69. Lau F.C.M., Chen G. Optimal layouts of midimew networks // IEEE Trans. Parallel Distrib. Syst. IEEE, 1996. Vol. 7, No. 9. P. 954–961. DOI: 10.1109/71.536939.

70. Zhang T.-Y., Ye D. Distributed Secure Control Against Denial-of-Service Attacks in Cyber-Physical Systems Based on K -Connected Communication Topology // IEEE Trans. Cybern. 2020. Vol. 50, No. 7. P. 3094–3103. DOI: 10.1109/TCYB.2020.2973303.

71. Erickson A. et al. The stellar transformation: From interconnection networks to datacenter networks // Comput. Networks. Elsevier, 2017. Vol. 113. P. 29–45. DOI: 10.1016/J.COMNET.2016.12.001.

72. Monahova E.A. Strukturnye i kommunikativnye svojstva cirkuljantnyh setej // Prikladnaja diskretnaja matematika. Novosibirsk, 2011. Vol. 3, No. 13. P. 92–115.

73. Monakhov O.G., Monakhova E.A. Regular Network Class Features Enhancement Using an Evolutionary Synthesis Algorithm // Science and Education of the Bauman MSTU. 2014. No. 10. P. 273–283. DOI: 10.7463/1014.0728878.

74. Monakhova E.A. A set of families of analytically described triple loop networks defined by a parameter // Prikl. Diskretn. Mat. 2020. No. 49. P. 108–119. DOI: 10.17223/20710410/49/8.

75. Monakhova E.A., Monakhov O.G. Construction of series of families of degree six circulant networks // Diskretnyi Analiz i Issledovanie Operatsii. 2022. Vol. 29, No. 4. P. 59–76. DOI: 10.33048/daio.2022.29.743.

76. Rzaev E.R., Romanov A.Y. Research of Promising Network-on-Chip Topologies: Application of Root and Direct Products of Paley Graphs // Problems of Perspective Micro- and Nanoelectronic Systems Development. 2021. No. 1. P. 9–16. DOI: 10.31114/2078-7707-2021-1-9-16.

77. Fatullaev A.F., Rzaev E.R., Romanov A.Y. Usage of Clustering of Paley Graphs in Polar Coordinates for the Development of New Network-on-Chip Topologies // 2022 International Russian Automation Conference (RusAutoCon). IEEE, 2022. P. 419–423. DOI: 10.1109/RusAutoCon54946.2022.9896241.

78. Rzaev E.R., Romanov A.Y. The New Promising Network-on-Chip Topologies Development Using Product Operation // 2021 International Russian Automation Conference (RusAutoCon). IEEE, 2021. P. 421–425. DOI: 10.1109/RusAutoCon52004.2021.9537317.

79. Loudiki L., Kchikech M., Essaky E.H. A new approach for computing the distance and the diameter in circulant graphs. 2022. DOI: 10.48550/arXiv.2210.11116.

80. Romanov A.Y., Romanova I.I., Glukhikh A.Y. Development of a Universal Adaptive Fast Algorithm for the Synthesis of Circulant Topologies for Networks-on-Chip Implementations // 2018 IEEE 38th International Conference on Electronics and Nanotechnology (ELNANO). IEEE, 2018. P. 110–115. DOI: 10.1109/ELNANO.2018.8477462.

81. Romanov A., Romanova I., Ivannikov A. Application of exhaustive search, branch and bound, parallel computing and Monte-Carlo methods for the synthesis of quasi-optimal network-on-chip topologies // 2017 IEEE East-West Design & Test Symposium (EWDTS). IEEE, 2017. P. 168–173. DOI: 10.1109/EWDTS.2017.8110092.

82. Rashodchikov M.Y., Romanov A.Y. Bibliotechnyj klass ScaNoC dlja sinteza kvazioptimal'nyh topologij setej na kristalle s zadannymi harakteristikami i ogranichenijami, Programm, 2016618167, 5.0262-2016.

83. Saldaña M., Shannon L., Chow P. The routability of multiprocessor network topologies in FPGAs // Proceedings of the internation symposium on Field programmable gate arrays - FPGA'06. NY, USA: ACM Press, 2006. P. 232. DOI: 10.1145/1117201.1117253.

84. Atajan T., Otsuka N., Yong X. Counting the number of spanning trees in a class of double fixed-step loop networks // Appl. Math. Lett. Pergamon. 2010. Vol. 23, No. 3. P. 291–298. DOI: 10.1016/j.aml.2009.04.006.

85. Beivide R. et al. Optimal Distance Networks of Low Degree for Parallel Computers // IEEE Trans. Comput. 1991. Vol. 40, No. 10. P. 1109–1124. DOI: 10.1109/12.93744.

86. Chen B., Xiao W., Parhami B. Diameter formulas for a class of undirected double-loop networks // J. Interconnect. Networks. WSPC, 2005. Vol. 06, No. 01. P. 1–15. DOI: 10.1142/S0219265905001289.

87. Zerovnik J., Pisanski T. Computing the Diameter in Multiple-Loop Networks // J. Algorithms. Academic Press, 1993. Vol. 14, No. 2. P. 226–243. DOI: 10.1006/jagm.1993.1011.

88. Loudiki L., Kchikech M., Essaky E.H. Diameter formulas for a class of undirected multi-loop networks. 2022. DOI: 10.48550/arXiv.2209.13018.

89. Dijkstra E.W. A note on two problems in connexion with graphs // Numer. Math. 1959. Vol. 1, No. 1. P. 269–271. DOI: 10.1007/BF01386390.

90. Hart P.E., Nilsson N.J., Raphael B. A Formal Basis for the Heuristic Determination of Minimum Cost Paths // IEEE Trans. Syst. Sci. Cybern. IEEE, 1968. Vol. 4, No. 2. P. 100–107. DOI: 10.1109/TSSC.1968.300136.

91. Abbott S., Bottcher A., Grudsky S.M. Toeplitz Matrices, Asymptotic Linear Algebra and Functional Analysis // Math. Gaz. 2000. Vol. 84, No. 501. P. 572. DOI: 10.2307/3620823.

92. Boesch F., Tindell R. Circulants and their connectivities // J. Graph Theory. 1984. P. 487–499. DOI: 10.1002/jgt.3190080406.

93. Romanov A.Y. et al. Analysis of Posit and Bfloat Arithmetic of Real Numbers for Machine Learning // IEEE Access. 2021. Vol. 9. P. 82318–82324. DOI: 10.1109/ACCESS.2021.3086669.

94. Miachin D.A. et al. The Open System for Storing and Processing of a Dataset of Combinational Circuits // Proc. Inst. Syst. Program. RAS. 2023. Vol. 35, No. 5. P. 81–90. DOI: 10.15514/ISPRAS-2022-35(5)-6.

95. Monakhova E.A., Monakhov O.G. Searching for record circulant graphs using a parallel genetic algorithm // Diskretnyi Analiz i Issledovanie Operatsii. 2015. Vol. 22, No. 6(126). P. 29–42. DOI: 10.17377/daio.2015.22.509.

96. Monakhova E.A., Monakhov O.G. Generation and Analysis of Optimal Double-Loop Circulant Networks Dataset // The 4th International Siberian Scientific Workshop on Data Analysis Technologies with Applications (SibDATA-2023). CEUR-WS, 2023.

97. Romanov A.Y., Vedmid E.V., Monakhova E.A. Designing Networks-on-Chip Based on Triple Loop (Circulant) Networks: Routing Algorithm Development // Information technologies. 2019. Vol. 25, No. 9. P. 522–530. DOI: 10.17587/it.25.522-530.

98. Hu W. et al. Open Graph Benchmark: Datasets for Machine Learning on Graphs // Adv. Neural Inf. Process. Syst. 2020. Vol. 33. P. 22118–22133. DOI: 10.48550/arXiv.2005.00687.

99. Sherwani N.A. Algorithms for VLSI physical design automation. Springer Science & Business Media, 2012.

100. Romashikhin M., Romanov A. Hardware-Software Complex for Prototyping NoCs Using a Few FPGA Chips // 2023 International Russian Automation Conference (RusAutoCon). IEEE, 2023. P. 330–334. DOI: 10.1109/RusAutoCon58002.2023.10272798.

101. Hesham S., Goehringer D., Abd El Ghany M.A. HPPT-NoC: A Dark-Silicon Inspired Hierarchical TDM NoC with Efficient Power-Performance Trading // IEEE Trans. Parallel Distrib. Syst. 2020. Vol. 31, No. 3. P. 675–694. DOI: 10.1109/TPDS.2019.2942589.

102. Wang K., Zheng H., Louri A. TSA-NoC: Learning-Based T hreat Detection and Mitigation for Secure Network-on-Chip Architecture // IEEE Micro. 2020. Vol. 40, No. 5. P. 56–63. DOI: 10.1109/MM.2020.3003576.

103. Tziantzioulis G. et al. OPDB: A Scalable and Modular Design Benchmark // IEEE Trans. Comput. Des. Integr. Circuits Syst. 2022. Vol. 41, No. 6. P. 1878–1887. DOI: 10.1109/TCAD.2021.3096794.

104. Santos M.C. et al. A Scalable Methodology for Agile Chip Development with Open-Source Hardware Components // Proceedings of the 41st IEEE/ACM International Conference on Computer-Aided Design. NY, USA: ACM, 2022. P. 1–9. DOI: 10.1145/3508352.3561102.

105. Romanov A.Y. et al. SAPR dlja vysokourovnevogo modelirovanija StnK (UHLNoCSim-SE), Program, 2023683151, 5.0018-2023.

106. Romanov A.Y., Ivannikov A.D., Romanova I.I. Simulation and synthesis of networks-on-chip by using NoCSimp HDL library // 2016 IEEE 36th International Conference on Electronics and Nanotechnology (ELNANO). IEEE, 2016. P. 300–303. DOI: 10.1109/ELNANO.2016.7493072.

107. Romanov A., Lezhnev E., Amerikanov A. Modification of the BookSim simulator for modeling networks-on-chip based on two-dimensional circulant topologies // CEUR Workshop Proceedings. CEUR-WS, 2019. Vol. 2514. P. 182–192.

108. Prilepko P.M., Romanov A.Y., Lezhnev E.V. Modification of a High-Level NoCModel 2.0 for Modeling Networks-on-Chip with Circulant Topologies // Problems of development of advanced micro- and nanoelectronic systems. 2020. No. 4. P. 23–20. DOI: 10.31114/2078-7707-2020-4-23-30.

109. Romanov A.Y. Universal'naja vysokourovnevaja programmnaja model' setej na kristalle Universal On-Chip Network Simulator (UOCNS), Program, 2019616754, 5.0318-2019.

110. Sukhov A.M., Romanov A.Y., Selin M.P. Virtual Coordinate System Based on a Circulant Topology for Routing in Networks-On-Chip // Symmetry (Basel). 2024. Vol. 16, No. 1. P. 127. DOI: 10.3390/sym16010127.

111. Romanov A.Y. et al. The Usage of a Simple SchoolMIPS Soft-Processor Core for Teaching Students the Computer Microarchitecture // 2022 International Conference on Quality Management, Transport and Information Security, Information Technologies (IT&QM&IS). IEEE, 2022. P. 382–387. DOI: 10.1109/ITQMIS56172.2022.9976796.

112. Markov D., Romanov A. Implementation of the RISC-V Architecture with the Extended Zbb Instruction Set // 2022 International Ural Conference on Electrical Power Engineering (UralCon). IEEE, 2022. P. 180–184. DOI: 10.1109/UralCon54942.2022.9906776.

113. Lezhnev E.V., Romanov A.Y. Generator Verilog koda podsistemy svjazi setej na kristalle (Verilog Code Generator of Communication Subsystem for Networks-on-Chip, HDLNoCGen), Program, 2021616623, 5.0064-2020.

114. Amerikanov A.A. et al. Development of Methods for Automating High-Level Modeling of Networks-on-Chip // Proceedings of the Institute for System Programming of the RAS (Proceedings of ISP RAS). 2023. Vol. 35, No. 5. P. 67–80. DOI: 10.15514/ISPRAS-2022-35(5)-5.

115. Flich J. et al. A survey and evaluation of topology-agnostic deterministic routing algorithms // IEEE Trans. Parallel Distrib. Syst. IEEE Computer Society, 2012. Vol. 23, No. 3. P. 405–425. DOI: 10.1109/TPDS.2011.190.

116. Kaleem M., Isnin I.F. A Survey on Network on Chip Routing Algorithms Criteria // Advances in Intelligent Systems and Computing. Springer Science and Business Media Deutschland GmbH, 2021. Vol. 1188. P. 455–466. DOI: 10.1007/978-981-15-6048-4_40.

117. Ahmad K., Sethi M. Review of network on chip routing algorithms // EAI Endorsed Trans. Context. Syst. Appl. 2020. Vol. 7, No. 22. P. 1–12. DOI: 10.4108/eai.23-12-2020.167793.

118. Verdoscia L., Vaccaro R. An Adaptive Routing Algorithm for WK-Recursive Topologies // Computing. 1999. Vol. 63, No. 2. P. 171–184. DOI: 10.1007/s006070050057.

119. Hafizur Rahman M.M., Horiguchi S. Routing performance enhancement in hierarchical torus network by link-selection algorithm // J. Parallel Distrib. Comput. 2005. Vol. 65, No. 11. P. 1453–1461. DOI: 10.1016/j.jpdc.2005.05.024.

120. Hu J., Marculescu R. Energy-aware mapping for tile-based NoC architectures under performance constraints // Proceedings of the Asia and South Pacific Design Automation Conference, ASP-DAC. Institute of Electrical and Electronics Engineers Inc., 2003. Vol. 2003-January. P. 233–239. DOI: 10.1109/ASPDAC.2003.1195022.

121. Monakhova E. et al. Optimal Routing Algorithm in Dense Gaussian Networks-on-Chip // 2022 International Conference on Electrical, Computer, Communications and Mechatronics Engineering (ICECCME). IEEE, 2022. P. 1–6. DOI: 10.1109/ICECCME55909.2022.9988159.

122. Monakhova E.A. On the analytical description of the optimal two-dimensional Diophantine structures of homogeneous computing systems // Comput. Syst. Quest. Theory Constr. Comput. Syst. 1981. Vol. 90. P. 81–91.

123. Stojmenović I. Multiplicative circulant networks topological properties and communication algorithms // Discret. Appl. Math. 1997. Vol. 77, No. 3. P. 281–305. DOI: 10.1016/S0166-218X(96)00138-2.

124. Shchegoleva M.A. et al. Routing in Networks on Chip with Multiplicative Circulant Topology // J. Phys. Conf. Ser. 2019. Vol. 1163. P. 012027. DOI: 10.1088/1742-6596/1163/1/012027.

125. Shchegoleva M.A., Romanov A.Yu. Development of Routing Algorithm in Networks-on-Chip with a Multiplicative Circulant Topology // Problems of development of advanced micro- and nanoelectronic systems. 2018. No. 3. P. 119–125. DOI: 10.31114/2078-7707-2018-3-119-125.

126. Monakhova E.A. et al. Analytical Routing Algorithm for Networks-on-Chip with the Three-dimensional Circulant Topology // 2020 Moscow Workshop on Electronic and Networking Technologies (MWENT). IEEE, 2020. P. 1–6. DOI: 10.1109/MWENT47943.2020.9067418.

127. Romanov A.Y., Sidorenko M.V., Lezhnev E.V. Routing in Networks-on-Chip with Circulant Topology with Three Generatrices of Type C(N; S1,S2,S3) // Proceedings - 2019 International Russian Automation Conference, RusAutoCon. 2019. DOI: 10.1109/RUSAUTOCON.2019.8867661.

128. Romanov A.Y., Vedmid' E.A. Programma marshrutizacii vyborom napravlenij v kol'cevyh cirkuljantah tret'ego porjadka, Program, 20196150135, 5.0030-2020.

129. Sidorenko M.V., Romanov A.Y. Programma marshrutizacii metodom delimosti linejnoj kombinacii obrazujushhih v cirkuljantah tret'ego porjadka, Program, 2019614803, 5.0051-2020.

130. Romanov A.Y., Sidorenko M.V., Monakhova E.A. Routing in Networks-on-Chip with a Three-Dimensional Circulant Topology // Information technologies. 2020. Vol. 26, No. 1. P. 22–29. DOI: 10.17587/it.26.22-29.

131. Robič B. Optimal routing in 2-jump circulant networks // Tech. Report N397. 1996. 7 p.

132. Dobravec T., Žerovnik J., Robič B. An optimal message routing algorithm for circulant networks // J. Syst. Archit. 2006. Vol. 52, No. 5. P. 298–306. DOI: 10.1016/j.sysarc.2005.12.003.

133. Žerovnik J., Robič B., Dobravec T. Optimal permutation routing in 2-jump circulant networks // Proc. 1st Int. Conf. Softw. Eng. Appl. Netw. Parallel/Distrib. Comput. (SNPD). 2000. P. 175–180.

134. Gómez D., Gutierrez J., Ibeas Á. Optimal routing in double loop networks // Theor. Comput. Sci. 2007. Vol. 381, No. 1–3. P. 68–85. DOI: 10.1016/J.TCS.2007.04.002.

135. Chen B.-X., Meng J.-X., Xiao W.-J. A Constant Time Optimal Routing Algorithm for Undirected Double-Loop Networks // Lecture Notes in Computer Science (Including subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics). Springer Verlag, 2005. Vol. 3794 LNCS. P. 308–316. DOI: 10.1007/11599463_31.

136. Martínez C. et al. Modeling toroidal networks with the Gaussian integers // IEEE Trans. Comput. 2008. Vol. 57, No. 8. P. 1046–1056. DOI: 10.1109/TC.2008.57.

137. Sukhov A.M., Romanov A.Y., Amerikanov A.A. The Problem of a Symmetric Graph with a Maximum Number of Vertices and Minimum Diameter // Lobachevskii J. Math. 2023. Vol. 44, No. 12. P. 5453–5459. DOI: 10.1134/S1995080223120351.

138. Moscibroda T. et al. Virtual coordinates for ad hoc and sensor networks // 2004 Joint Workshop on Foundations of Mobile Computing. Association for Computing Machinery (ACM), 2004. P. 8–16. DOI: 10.1145/1022630.1022633.

139. Lim H., Lim C., Hou J.C. A coordinate-based approach for exploiting temporal-spatial diversity in wireless mesh networks // Annual International Conference on Mobile Computing and Networking. Association for Computing Machinery (ACM), 2006. P. 14–25. DOI: 10.1145/1161089.1161093.

140. Dhanapala D.C., Jayasumana A.P. Anchor selection and topology preserving maps in WSNs - A Directional virtual coordinate based approach // Conference on Local Computer Networks. 2011. P. 571–579. DOI: 10.1109/LCN.2011.6115519.

141. Gaidamaka Y., Samouylov K. UVCS: Unit Virtual Coordinate System for UAV Intra-Swarm Routing in GPS-Denied Environment // Mathematics. 2023. Vol. 11, No. 3. P. 694. DOI: 10.3390/math11030694.

142. Sukhov A.M., Romanov A.Y., Glushak E.V. Routing in circulant graphs based on a virtual coordinate system // Uchenye Zapiski Kazanskogo Universiteta. Seriya Fiziko-Matematicheskie Nauki. 2024. Vol. 165, No. 3. P. 282–293. DOI: 10.26907/2541-7746.2023.3.282-293.

143. Das S., Karfa C., Biswas S. Formal Modeling of Network-on-Chip Using CFSM and its Application in Detecting Deadlock // IEEE Trans. Very Large Scale Integr. Syst. IEEE, 2020. Vol. 28, No. 4. P. 1016–1029. DOI: 10.1109/TVLSI.2019.2959618.

144. Park D. et al. Exploring fault-tolerant network-on-chip architectures // International Conference on Dependable Systems and Networks. 2006. P. 93–104. DOI: 10.1109/DSN.2006.35.

145. Cheng D.W., Yao K.H., Hsieh S.Y. Constructing Independent Spanning Trees on Generalized Recursive Circulant Graphs // IEEE Access. Institute of Electrical and Electronics Engineers Inc., 2021. Vol. 9. P. 74028–74037. DOI: 10.1109/ACCESS.2021.3080315.

146. Myachin N.M., Romanov A.Yu., Monakhova E.A. Deadlock-Free Routing in Networks-on-Chip with Circulant Topologies // Problems of development of advanced micro- and nanoelectronic systems. 2021. No. 3. P. 99–105. DOI: 10.31114/2078-7707-2021-3-99-105.

147. Masone A. et al. The Minimum Routing Cost Tree Problem: State of the art and a core-node based heuristic algorithm // Soft Comput. Springer Verlag, 2019. Vol. 23, No. 9. P. 2947–2957. DOI: 10.1007/s00500-018-3557-3.

148. Dally W.J., Seitz C.L. Deadlock-Free Message Routing in Multiprocessor Interconnection Networks // IEEE Trans. Comput. 1987. Vol. C–36, No. 5. P. 547–553. DOI: 10.1109/TC.1987.1676939.

149. Biss D.K. Hamiltonian decomposition of recursive circulant graphs // Discrete Math. 2000. Vol. 214, No. 1–3. P. 89–99. DOI: 10.1016/S0012-365X(99)00199-5.

150. Dean M. On Hamilton Cycle Decomposition of 6-regular Circulant Graphs // Graphs Comb. 2006. Vol. 22, No. 3. P. 331–340. DOI: 10.1007/s00373-006-0657-0.

151. Alspach B., Dyer D., Kreher D.L. On isomorphic factorizations of circulant graphs // J. Comb. Des. 2006. Vol. 14, No. 5. P. 406–414. DOI: 10.1002/jcd.20080.

152. El-Mesady A. et al. On Orthogonal Double Covers and Decompositions of Complete Bipartite Graphs by Caterpillar Graphs // Algorithms. 2023. Vol. 16, No. 7. P. 320. DOI: 10.3390/a16070320.

153. El-Mesady A., Hamed Y.S., Shabana H. On the decomposition of circulant graphs using algorithmic approaches // Alexandria Eng. J. Elsevier, 2022. Vol. 61, No. 10. P. 8263–8275. DOI: 10.1016/J.AEJ.2022.01.049.

154. Lisitsyna M.A., Parshina O.G. Perfect colorings of the infinite circulant graph with distances 1 and 2 // J. Appl. Ind. Math. 2017. Vol. 11, No. 3. P. 381–388. DOI: 10.1134/S1990478917030097.