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Integrated Circuit of an Intelligent Reflecting Surface for sub-THz Wireless Communication

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***Abstract*—Next-generation networks demand efficient hardware solutions for wireless communication channels with carrier frequencies beyond 100 GHz. In particular, beamforming in reflected light is suggested to reduce signal attenuation due to blockages and to enhance overall quality of a wireless connection. This task can be solved with the aid of a network of intelligent reflecting surfaces placed in optical path between transmitter and receiver. In this work, we propose design of such a surface operated at 140 GHz which is fully compatible with clean room fabrication processes.**

***Index Terms*—Integrated circuit, intelligent reflecting surface, 6G network, wireless channel, sub-terahertz communication**

I. Introduction

Sixth-generation (6G) networks demand new hardware solutions for low-loss distribution of electromagnetic (EM) waves at carrier frequencies of 100 GHz or even higher. Routing of narrow transmitted beams is considered effective in terms of both propagation losses and multibeam interference. This task can be solved with the aid of a network of intelligent reflecting surfaces (IRSs) placed in optical path between transmitter and receiver. As suggested by its name, IRS is used for beamforming in reflected light which is achieved by adjusting locally the phase shift upon reflection of incident EM wave.

Few designs of digital phase shifters for millimeter wave (mmWave) IRSs have been proposed. Alternating current (AC) control designs with 1- and 2-bit resolution of elements operated at 76.5 GHz [1] and 28.5 GHz [2] are among them. In these designs, switches are used to alter distribution of currents in slotted metallic screen inserted in between of front and rear metallization patterns of a patch antenna array. Both the screen and the patterns are implemented on thin dielectric substrates with relative permittivities of 3.5–4.5, the substrates are spaced by air gaps. Such a geometry imposes tight requirements on mechanical parts in the IRS assembly if scaled down for 140 GHz operation. Moreover, the designs rely on either microelectromechanical system (MEMS) or PIN diode switches which potentially compromises their performance at 140 GHz.

In this work, we propose design of a sub-terahertz (sub-THz) IRS fully compatible with clean room fabrication pro-

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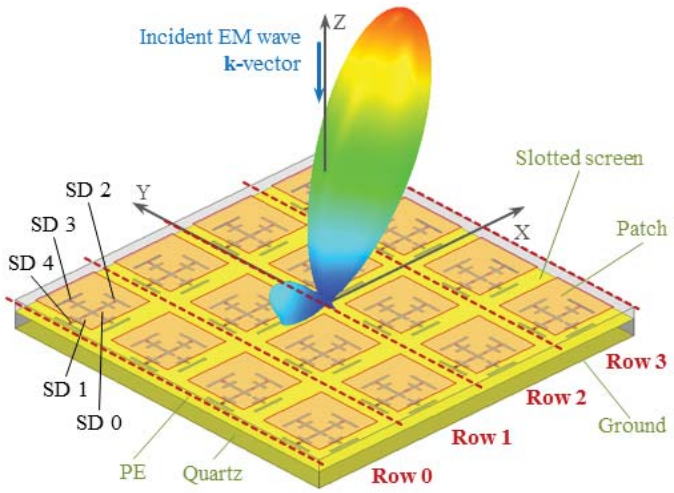

Fig. 1. A 3D model of the proposed sub-THz IRS with a profile of reflected Gausssian beam.

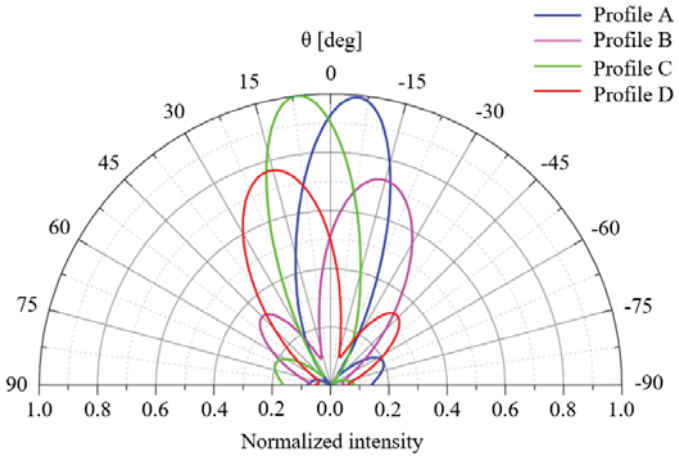

Fig. 2. Profiles of Gausssian beams reflected from sub-THz IRSs with different states of phase shifters in each row. Calculated at 135 GHz

cesses. A 3-dimensional (3D) model of the proposed IRS along with details on EM design and fabrication considerations are provided further in the text.

II. EM Design and Fabrication Considerations

As a preliminary design, we have developed an IRS suitable for operation at 130–140 GHz and inspired by that described in [2], i.e., making use of AC control in slotted metallic screen inserted in between of front and rear metallization patterns of a patch antenna array [3]. The developed IRS consists of 16 phase shifters organized in a planar array and is capable of a multi-state beamforming. The patches and the slotted screen integrated with Schottky diode switches for current control are implemented on 2 separate crystalline quartz substrates with linear dimensions of $1.6\lambda_0 \times 1.6\lambda_0 \times 0.012\lambda_0$ (length $\times$ width $\times$ height). The substrates are spaced by an air gap of $0.02\lambda_0$. Here λ_0 is the wavelength of EM radiation in vacuum. Ground plane of the patch antenna array can be implemented directly on a back surface of the substrate with the slotted screen or at a $0.25\lambda_0$ distance behind it. In the latter case, beamforming capabilities of the IRS are enhanced, but complexity of the IRS assembly is significantly increased.

A. EM Design

To make the preliminary design of a sub-THz IRS compatible with clean room fabrication processes, we first decide to eliminate the air gaps in its mechanical structure. Fig. 1 provides a 3D model of the updated IRS acquired via EM simulations.

Referring to Fig. 1, the thickness of the lower fused quartz substrate equals 150 μm, and the upper substrate is presented by a 100 μm thick polyethylene (PE). Geometries of the patches, the slotted screen and the positioning of the diode switches remain unchanged as compared to the preliminary design of IRS described earlier in Sec. II.

TABLE I
Phase Shifter States.

State	DC Bias of Schottky Diodes					S-parameters[a]	
#	SD 0	SD 1	SD 2	SD 3	SD 4	mag($S11$) [dB]	arg($S11$) [deg]
0	$\hat{Z}_F$	$\hat{Z}_0$	$\hat{Z}_0$	$\hat{Z}_0$	$\hat{Z}_0$	-1.21	106.8
1	$\hat{Z}_F$	$\hat{Z}_0$	$\hat{Z}_F$	$\hat{Z}_F$	$\hat{Z}_F$	-1.50	17.7

[a]Calculated at 135 GHz

The performed in HFSS EM simulations include the Floquet port and incident wave analyses. They are used to calculate a) parameters of phase shifters and b) profiles of Gausssian beams reflected from IRSs with different states of phase shifters in each row. Schottky diodes (SDs) are implemented as squares with sheet impedances $\hat{Z}_0 \approx 3.1 - 189.6i\ \Omega/\square$ and $\hat{Z}_F \approx 3\ \Omega/\square$ for modeling the impact of a nearly zero and high forward direct current (DC) bias voltages, respectively. Results of the EM simulations are provided below.

Tab. I summarizes parameters of a phase shifter in 2 different states defined by DC biasing of its Schottky diodes. As one can clearly see, the magnitude of the reflected wave is not drastically affected by the change of the phase shifter state. And the magnitude of $S11$ stays around -1.35 dB in both cases. In turn, the phase of $S11$ varies by 89.1 deg. This feature is used to implement different configurations of a sub-THz IRS upon beamforming.

Fig. 2 provides profiles of Gausssian beams reflected from sub-THz IRSs with different states of phase shifters in each row. Profile A is acquired for IRS with rows 0 and 2 in state 0, and rows 1 and 3 in state 1. Profile B is acquired for IRS with rows 0 and 1 in state 0, and rows 2 and 3 in state 1. Profile C is acquired for IRS with rows 0 and 2 in state 1, and rows 1 and 3 in state 0. Profile D is acquired for IRS with rows 0 and 1 in state 1, and rows 2 and 3 in state 0. The distribution

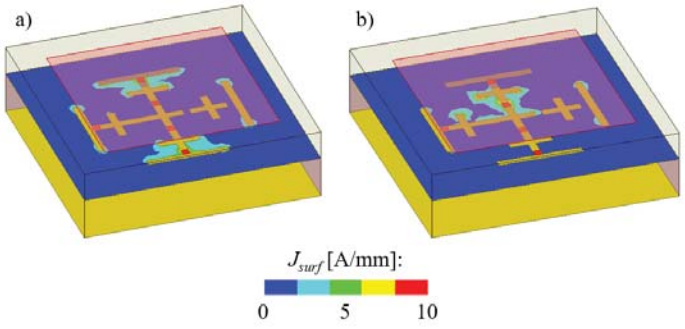

Fig. 3. Surface current density in a slotted screen for a) phase shifter in state 0 and b) phase shifter in states 1.

of a surface current density in the phase shifter slotted screen, J_{surf}, as a function of its bias state is provided in Fig. 3.

It is worth mentioning that all beam profiles and current distributions are calculated in case of the normal incidence of a sub-THz wave. However, the developed design potentially enables beamforming for various angles of incidence. And the presence of 5 Schottky diodes in each phase shifter ensures 2-bit phase resolution upon reflection. This relies on an out-of-phase bias change of SD 0 and SD 1, and an in-phase bias change of SD 2 – SD 4. Only 2 DC bias lines per row are required which simplifies fabrication noticeably.

B. Fabrication Considerations

First step is to fabricate slotted screen integrated with Schottky diodes. The fabrication includes deposition and patterning of metallization systems of cathode and anode contacts, structuring of a GaAs-based heterostructure grown by the means of molecular beam epitaxy. Baseline is described in details elsewhere [4]. GaAs wafer is further flip-chip bonded to front surface of a back-metallized 150 μm thick quartz substrate, i.e., in front of a ground plane of patch antenna array. Area of the quartz substrate is chosen such that precise alignment is not required in the process. Semi-insulating (SI) GaAs handle is further removed by wet chemical etching. Isolated traces for DC biasing are fabricated on top of a SiO_2-coated etch-stopper of the heterostructure and electrically connected to Schottky diodes through preliminary etched openings in it.

Next step is to fabricate metallic patches on a 100 μm thick PE placed on top of the fabricated slotted screen. For this task, we propose two alternative options. One option is related to the use of a regular low-density PE film. The film is placed on the slotted screen under low and uniformly distributed pressure. The structure is warmed up to a temperature close to the PE melting point for a short time and slowly cooled down. Alternatively, special heat-activated adhesive nonconductive film, e.g., Loctite Ablestik NCF from Henkel, may be used instead of low-density PE. In both cases, heat treatment is performed in nitrogen atmosphere. Deposition and patterning of the metallic patches on the deposited PE film are further performed.

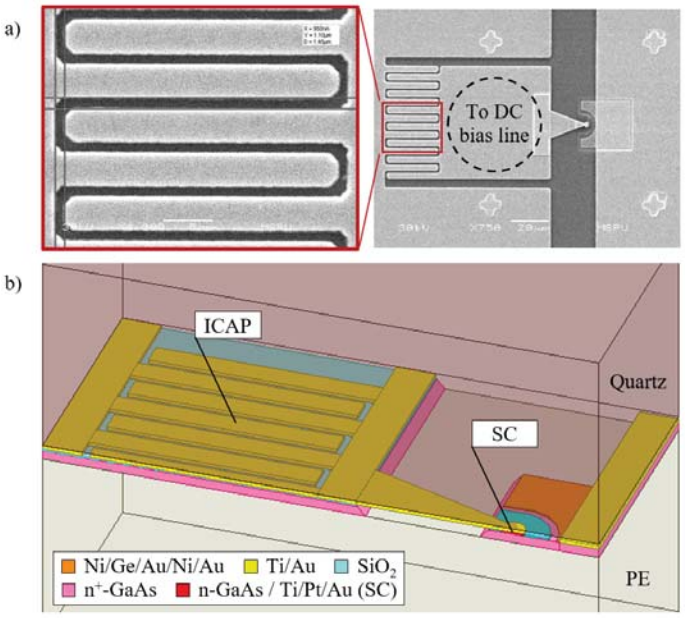

Fig. 4. An ICAP-integrated Schottky diode with a triangular anode suspended bridge: a) SEM image of the fabricated structure and b) its EM model.

TABLE II
LAYERED STRUCTURE OF A PLANAR SCHOTTKY DIODE.

Layer #	Composition[a]	Thickness
1	Ti/Au	5/450 nm – 5/500 nm
2	Ni/Ge/Au/Ni/Au	50/20/35/15/80 nm
3	Ti/Pt/Au	50/20/20 nm
4	SiO_2	250 nm
5	Si-doped n-GaAs (N_d)	190 nm
6	Si-doped n^+-GaAs (N_{d+})	2 μm
7	SI-GaAs(100) substrate	630 μm

[a]Dopant levels $N_d = 3.9 \times 10^{17}$ cm^{-3} and $N_{d+} = 5.1 \times 10^{18}$ cm^{-3}

C. Prototyping and Feasibility Assessment

To integrate Schottky diodes with DC bias lines and not to disturb AC currents in phase shifters, we plan to implement interdigital capacitors (ICAPs) [5] between the anode of each diode and the IRS slotted screen. All cathodes are to be connected to the slotted screen directly. A scanning electron microscope (SEM) image of an ICAP-integrated Schottky diode, which we fabricate at our clean room facility, is provided in Fig. 4(a).

Tab. II describes the layered structure of fabricated planar Schottky diodes. We use epitaxially grown GaAs wafers. Schottky contact (SC) to n-GaAs is maintained by a Ti/Pt/Au rod through a circular opening in SiO_2. Ohmic contact to n^+-GaAs is formed using a Ni/Ge/Au/Ni/Au metallization system, the layered structure is exposed to rapid thermal annealing.

Fig. 4(a) also provides a zoomed-in image of the interdigital capacitor fingers with gap between them. The gap widths of

0.95 and 1.1 μm are measured along 2 mutually perpendicular directions which are close to the nominal value of 1 μm. We choose such a gap width, w_g, to make the capacitor fabrication compatible with photolithography-assisted processes. This, in turn, raises the question whether its resulting capacitance is sufficient for proper operation of IRS or not. Moreover, the fabricated diodes have rather large triangular anode suspended bridges to improve their mechanical reliability. This is quite important since flip-chip mounting of substrate with Schottky diodes is considered as a part of the IRS fabrication process. Removal of n- and n^+-GaAs layers under the bridge aids to reduce parasitic capacitive coupling between the diode structural elements. However, we decide not to remove n^+-GaAs underneath the ICAP area, but to isolate it by thin SiO_2 layer. This leads to the appearance of additional conductor with an electric potential different from those of the ICAP fingers. Therefore, the resulting capacitance, C_{icap}, of such a 'grounded' interdigital capacitor should grow. It is now determined not only by the width and length of the ICAP fingers and the gap between them, but also by the thickness of the SiO_2 layer, t_d. Extraction of the implementation-dependent LC-parameters of the developed ICAP-integrated Schottky diode via EM simulations is further discussed.

The ABCD-parameters matrix, a, of a two-port lumped LC-circuit with impedance, $\hat{Z}_{LC}$, connected in series with two electrically short transmission lines is defined by Eq. 1. The corresponding Y-parameters matrix obeys Eq. 2, where $Y[1,2] = -\hat{Z}_{LC}^{-1}$.

$$a \approx \begin{bmatrix} 1 & \hat{Z}_{LC} \\ 0 & 1 \end{bmatrix} \tag{1}$$

$$Y = \frac{1}{a[1,2]} \begin{bmatrix} a[2,2] & -|a| \\ -1 & a[1,1] \end{bmatrix} \tag{2}$$

$$C_{icap} = \left(2\pi F \, im \left(\frac{1}{Y[1,2]} - \frac{1}{Y_{cal}[1,2]} \right) \right)^{-1} \tag{3}$$

Fig. 4(b) illustrates EM model of an ICAP-integrated planar Schottky diode placed between quartz and polyethylene substrates. This setup acts as the inner wire of an air-filled coaxial transmission line with the outer shell radius of 245 μm. The transmission line is excited by 2 wave ports, the symmetry plane boundary is used to improve the simulation time efficiency. All metals and semiconductors are modeled as perfect conductors, losses in dielectrics are neglected. We calculate C_{icap} at frequency F in accordance with Eq. 3, where $Y_{cal}[1,2]$ denotes Y-parameter calculated in case of the short-circuited and collapsed ICAP. This is achieved by a) defining the SiO_2 layer under ICAP as a perfect conductor, b) reducing the ICAP finger length and the spacing from it to anode suspended bridge to 0.1 μm. We acquire C_{icap} values of 202 and 91.1 fF for t_d equal to 50 and 250 nm, respectively. This results in the ICAP reactance of 5.8–12.9 Ω, which can be easily reduced to 1 Ω upon further decrease in w_g and t_d. Moreover, minor tuning of the diode planar structure can provide both zero-bias capacitance of a Schottky contact $C_{j0} \approx 1$ fF and total shunt capacitance $C_{tot} \approx 5$ fF considered earlier in Sec. II-A. Series resistance $R_s \approx 3\,\Omega$ is also feasible if ideality factor is sacrificed [6].

For justification of both the EM design and first-run clean room processes, we plan to fabricate and study a series of IRSs with simplified structure. Schottky diodes are going to be replaced by shorts or opens depending on configuration of IRS. In this case, both the slotted screen and the ground plane of patch antenna array can be implemented on a quartz substrate during the first step of the fabrication process. Our preliminary studies of V/Cu films deposited on PE-coated quartz reveal a) position-dependent PE thickness of 94.4 ± 3.7 μm, b) decent adhesion (0 points out of 6 [7]) of V/Cu to PE, c) sheet resistance of V/Cu (10/200 nm) film of $0.148 \pm 0.025\,\Omega/\square$. This justifies feasibility of using PE coating with deposited on it V/Cu patches in the integrated circuit of a sub-THz IRS. Thus, we further plan to fabricate the integrated circuit and to study its performance. Prior to beam profile measurements, changes in performance are going to be forecasted by additional EM simulations.

III. Conclusion

In this work, we propose design of a sub-THz intelligent reflecting surface fully compatible with clean room fabrication processes. It relies on a modified patch antenna array, in which a slotted metallic screen with Schottky diodes for current control is inserted in between of front and rear metallization patterns. The patches and the slotted screen are implemented on a polyethylene-coated quartz substrate. Not-so-ideal planar diodes with a microscale Schottky contact and low series resistance ensure reflection losses of 1.2–1.5 dB and a 2-bit phase resolution in a unit cell upon reflection. 'Grounded' interdigital capacitor is used for AC coupling of each diode with the slotted screen and for its isolation upon DC biasing. The developed intelligent reflecting surface consists of 16 unit cells organized in a planar array and is capable of a multi-state beamforming. Only 2 DC bias lines per row are required which simplifies fabrication noticeably. We assess feasibility of the proposed design by both numerical simulations and prototyping. We believe that our findings will be of use in the development of wireless systems for 6G communication networks.

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